

INTEGRATED CIRCUITS AND APPILATIONS LABORATORY MANUAL (ECE - 318) III/IV ECE SEM - I



**By
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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

ANIL NEERUKONDA INSTITUTE OF TECHNOLOGY & SCIENCES (A)
(Affiliated to AU, Approved by AICTE & Accredited by NBA)
Sangivalasa-531 162, Visakhapatnam District,
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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
Anil Neerukonda Institute of Technology & Sciences (Autonomous)
Sangivalasa-531 162, Bheemunipatnam Mandal, Visakhapatnam District

Vision of the Institute

ANITS envisions to emerge as a world-class technical institution whose products represent a good blend of technological excellence and the best of human values.

Mission of the Institute

To train young men and women into competent and confident engineers with excellent communication skills, to face the challenges of future technology changes, by imparting holistic technical education using the best of infrastructure, outstanding technical and teaching expertise and an exemplary work culture, besides molding them into good citizens

Vision of the Department

To become a centre of excellence in Education, research and produce high quality Engineers in the field of Electronics and Communication Engineering to face the challenges of future technological changes.

Mission of the Department

To achieve vision department will

Transform students into valuable resources for industry and society by imparting contemporary technical education.

Develop interpersonal skills and leadership qualities among students by creating an ambience of academic integrity to participate in various professional activities

Create a suitable academic environment to promote research attitude among students.



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Program Educational Objectives (PEOs):

PEO1 : Graduates excel in their career in the domains of Electronics, Communication and Information Technology.

PEO2 : Graduates will practice professional ethics and excel in professional career through interpersonal skills and leadership qualities.

PEO3 : Graduates demonstrate passion for competence in higher education, research and participate in various professional activities.

Program Outcomes (POs):

Engineering Graduates will be able to:

1. **Engineering knowledge:** Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.
2. **Problem analysis:** Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.
3. **Design/development of solutions:** Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.
4. **Conduct investigations of complex problems:** Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.
5. **Modern tool usage:** Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.
6. **The engineer and society:** Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.
7. **Environment and sustainability:** Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.
8. **Ethics:** Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.
9. **Individual and team work:** Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.
10. **Communication:** Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.

11. **Project management and finance:** Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.
12. **Life-long learning:** Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

Program Specific Outcomes (PSOs):

- PS01 :** Implement Signal & Image Processing techniques using modern tools.
- PS02 :** Design and analyze Communication systems using emerging techniques.
- PS03 :** Solve real time problems with expertise in Embedded Systems.

INTEGRATED CIRCUITS LABORATORY	
ECE318	Credits:2
Instruction: 3 Lab periods	Sessional Marks:50
End Exam: 3 Hours	End Exam Marks:50

COURSE OUTCOMES

At the end of the course student will be able to	
1.	Design the circuits using op-amps for various applications like Schmitt Trigger, Precision Rectifier, Comparators and three terminal IC 78XX regulator.
2.	Design active filters for the given specifications and obtain their frequency response characteristics.
3.	Design and analyze multivibrator circuits using op-amp and 555Timer
4.	Design and analyze various combinational circuits like multiplexers, and de-multiplexers, binary adder, subtractor, etc
5.	Design and analyze various sequential circuits like flip-flops, counters etc

Mapping of Course Outcomes with Program Outcomes:

		PO												PSO			
		1	2	3	4	5	6	7	8	9	10	11	12	1	2	3	
CO	1	2	2	2	3	1	-	-	1	1	1						2
	2	2	2	2	3	1	-	-	1	1	1						2
	3	2	2	2	3	1	-	-	1	1	1						2
	4	2	2	2	3	1	-	-	1	1	1						2
	5	2	2	2	3	1	-	-	1	1	1						2

3: high correlation, 2: medium correlation, 1: low correlation

List of Experiments:

S.No	List of Experiments	Page No
1	Application of Operational Amplifiers	01
2	Design and testing of Active LPF & HPF using op-amp	08
3	Design of Schmitt Trigger using op-amp	18
4	Design of Astable multivibrator using a) op amp b) IC555	23
5	Line and load regulation of three terminal IC Voltage Regulator	34
6	Operation of R-2R ladder DAC and flash type ADC	39
7	Simulation of any 4 Experiments 1, 2, 3, 4, 5 and 6 using Multisim software	-
8	Minimization and Realization of a given Function using Basic Gates (AND, OR, NOR, NAND, EXOR).	44
9	Design and implementation of code converters using logic gates (i) BCD to excess-3 code (ii) Gray to binary	51
10	Design of binary adder and subtractor	57
11	Design and implementation of Multiplexer and De-multiplexer using logic gates	62
12	Implementation and Testing of RS Latch and Flip-flops – D, JK and T	68
13	Design of synchronous counters	77
14	Design of asynchronous counters	82

Note: A student has to perform a minimum of 12 experiments.



Scheme of Evaluation
(INTEGRATED CIRCUITS LABORATORY)

Total marks for each student to evaluate in lab: 100 marks

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Out of 100 marks:

- 1. External exam Evaluation : 50marks**
- 2. Internal Evaluation : 50 marks**
 - i. Internal exam : 25marks**
 - ii. Continuous Evaluation : 25 marks**

1. Internal Evaluation (50M)

i. Continuous Evaluation(25M)

- I. Preparation of Observation – 5M**(The appropriate aim, experimental design, Circuit diagram , selection of components, & Model Graph)
- II. Execution of Experiment/Result – 5M**(The procedure of doing experiment, Apparatus usage& accurate Output(Theoretical & Practical correlation), valid Result Statements)
- III. Record – 5M** (The record submitted in time and with neat & clear(Write-up,Aim,Appratus,Procedure,Theory), Circuit diagram, Experimental design, Graphs & valid Result Statements)
- IV. Pre lab & Post lab questions – 5M**(The number of questions answered before and after doing the each lab experiment)
- V. Attendance ---- 5M**

ii. Internal End Exam – 25M

(Write up – 10M, Performance – 5M , Result/Graph – 5M, Viva – 5M)

2. External exam Evaluation: (50M)

- I. Write up – 5M**
- II. Design /Circuit Diagram – 15M**
- III. Experiment/Output – 10M**
- IV. Result/Graph – 10M**
- V. Viva – 10M**

IC Applications Laboratory Assessment Rubric

Rubrics for Linear IC Design experiments

<i>Scheme</i>	<i>Excellent (5M)</i>	<i>Good(3M)</i>	<i>Average(2M)</i>	<i>Poor(1M)</i>
Preparation of observation (max:5M)	Maximum marks are given if the appropriate aim, experimental <i>design</i> , <i>Circuit diagram</i> , selection of components, & <i>Model Graph (Correct in all the aspects)</i>	Maximum marks are given if the appropriate aim, in correct experimental <i>design</i> , <i>Circuit diagram</i> , selection of components, & <i>Model Graph</i>	Maximum marks are given if the appropriate aim, incorrect experimental <i>design</i> , incorrect <i>Circuit diagram</i> , selection of components, & incorrect <i>Model Graph</i>	Maximum marks are given if the appropriate aim, experimental <i>design</i> , <i>Circuit diagram</i> , selection of components, & <i>Model Graph (incorrect in all the aspects)</i>
Execution of experiment/Results (max:5M)	Maximum marks are given if the procedure of doing experiment, <i>Apparatus usage</i> & accurate Output(Theoretical & Practical correlation), valid Result Statements (Correct in all the aspects)	Maximum marks are given if the procedure of doing experiment, <i>Apparatus usage</i> & not accurate Output(Theoretical & Practical correlation), valid Result Statements	Maximum marks are given if the procedure of doing experiment, <i>Apparatus usage</i> & not accurate Output(Theoretical & Practical correlation), invalid Result Statements	Maximum marks are given if the procedure of doing experiment, <i>Apparatus usage</i> & accurate Output(Theoretical & Practical correlation), Valid Result Statements (incorrect in all the aspects)
Record (max:5M)	Maximum marks are given if the record submitted in time and with neat & clear(Write-up(Aim,Appratus,Procedure, Theory), <i>Circuit diagram</i> , Experimental design, Graphs & valid Result Statements) (Correct in all the aspects)	Maximum marks are given if the record submitted in time and without neat & clear(Write-up(Aim,Appratus,Proced ure,Theory), <i>Circuit diagram</i> , Experimental design, Graphs & valid Result Statements)	Maximum marks are given if the record submitted in time and without neat & clear(Write-up(Aim,Appratus,Pro cedure,Theory), <i>Circuit diagram</i> , Experimental design, Graphs & invalid Result Statements)	Maximum marks are given if the record submitted not in time and without neat & clear(Write-up(Aim,Appratus,Pro cedure,Theory), <i>Circuit diagram</i> , Experimental design, Graphs & invalid Result Statements)
Pre-lab and Post lab questions(max:5M)	As per the number of questions answered before and after doing the each lab experiment	As per the number of questions not answered before and answered after doing the each lab experiment	As per the number of questions partially answered before and after doing the each lab experiment	As per the number of questions not answered before and after doing the each lab experiment

Rubrics for Digital Design experiments

<i>Scheme</i>	<i>Excellent (5M)</i>	<i>Good(3M)</i>	<i>Average(2M)</i>	<i>Poor(1M)</i>
Preparation of observation (max:5M)	Maximum marks are given if the appropriate aim, Logic design, <i>Logic diagram with optimization of gate count</i> , selection of Digital ICs and their <i>Pin Diagram & Truth Table</i> (Correct in all the aspects)	Maximum marks are given if the appropriate aim, correct logic design, <i>logic diagram without optimization of gate count</i> , selection of Digital ICs and their <i>Pin Diagram & Truth Table</i>	Maximum marks are given if the appropriate aim, in correct logic design, <i>logic diagram without optimization of gate count</i> , selection of Digital ICs and their <i>Pin Diagram & Truth Table</i>	Maximum marks are given if the appropriate aim, logic design, <i>logic diagram, optimization of gate count</i> , selection of Digital ICs and their <i>Pin Diagram & Truth Table</i> (incorrect in all the aspects)
Execution of experiment/Results (max:5M)	Maximum marks are given if the procedure of doing experiment, selection of components & accurate Output(Truth Table Verification), Valid Result Statements (Correct in all the aspects)	Maximum marks are given if the procedure of doing experiment, selection of components & not accurate Output(Truth Table Verification), valid Result Statements	Maximum marks are given if the procedure of doing experiment, selection of components & accurate Output(Truth Table Verification), invalid Result Statements	Maximum marks are given if the procedure of doing experiment, selection of components & accurate Output(Truth Table Verification), Valid Result Statements (incorrect in all the aspects)
Record(max:5M)	Maximum marks are given if the record submitted in time and with neat & clear(Write-up(Aim,Appratus,Procedure,Theory), Logic diagram, Pin Diagram Design& Truth Table, valid Result Statements) (Correct in all the aspects)	Maximum marks are given if the record submitted in time and without neat & clear(Write-up(Aim,Appratus,Procedure,Theory), Logic diagram, Pin Diagram Design& Truth Table, valid Result Statements)	Maximum marks are given if the record submitted in time and without neat & clear(Write-up(Aim,Appratus,Procedure,Theory), Logic diagram, Pin Diagram Design& Truth Table, invalid Result Statements)	Maximum marks are given if the record submitted in time and with neat & clear(Write-up(Aim,Appratus,Procedure,Theory), Logic diagram, Pin Diagram Design& Truth Table, valid Result Statements) (incorrect in all the aspects)
Pre-lab and Post lab questions(max:5M)	As per the number of questions answered before and after doing the each lab experiment	As per the number of questions not answered before and answered after doing the each lab experiment	As per the number of questions partially answered before and after doing the each lab experiment	As per the number of questions not answered before and after doing the each lab experiment

Note: Average of cycle I and Cycle II for a maximum of 20Marks

LAB PHOTO





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LIST OF MAJOR EQUIPMENT IN (ANALOG / DIGITAL) COMMUNICATION LABORATORY

SL.NO	NAME OF THE EQUIPMENT	MAKE	QUANTITY
1.	50 MHZ DIGITAL STORAGE OSCILLOSCOPE	TEKTRONICS	12
2.	0-30V REGULATED POWER SUPPLY	ITL /FALCON/APLAB	14
3.	1MHZ FUNCTION GENERATOR	APLAB	07
4.	20 MHZ DUAL TRACE OSCILLOSCOPE	CADO	04
5.	3KVA ONLINE UPS	MEGAPOWER	01
6.	BLOCK CODE ENCODER&DECODER	SCIEN TECH	02
7.	CONVOLUTION CODE ENCODER&DECODER	SCIEN TECH	02
8.	ACL-AMPLITUDE MODULATION&DEMODULATION	AKADEMIKA LAB SOLUTIONS	02
9.	PL-DSP TRAINER KIT	AKADEMIKA LAB SOLUTIONS	02
10.	PERSONAL COMPUTER SYSTEM	HCL	06
11.	SPECTRUM ANALYZER	AGILENT TECHNOLOGIES PVT.LIMITED	01

TOTAL EXPENDITURE OF THE LABORATORY(including consumables) :Rs27,79,409.37/-



Integrated Circuits And Applications Laboratory

Do's

1. Be punctual and regular to the laboratory.
2. Maintain Discipline all the time and obey the instructions.
3. Read and understand how to carry out an experiment thoroughly before coming to the laboratory.
4. Check the connections properly before turning ON the circuit.
5. Turn OFF the circuit immediately if you see any component heating.
6. Dismount all the components and wires before returning the kit.
7. Report any broken plugs/apparatus or exposed electrical wires to the faculty member/laboratory technician immediately.
8. Shut down the systems properly

Don'ts

1. Don't touch live electric wires.
2. Don't turn ON the circuit unless it is completed.
3. Avoid making loose connections.
4. Do not remove anything from the kits/experimental set up without permission.
5. Do not handle any equipment without reading the instructions/Instruction manuals
6. Don't leave the lab without permission.

1. Application of Operational Amplifiers

Aim:

To realize the following op-amp applications:

- (i) Precision Rectifier
- (ii) Inverting and Non-inverting Comparator
- (iii) Zero Crossing Detectors

Precision Rectifier

Pre – Requisites:

The student should have completed the following study before doing this experiment

- Op-amp theory and characteristics
- Inverting and non-inverting amplifiers

Pre – lab Questions:

1. The rectifying voltage amplitude in a precision rectifier is typically
a) Tens of volts b) a few volts **c) a few mill volts** d) microvolt's
2. The precision rectifier achieves functionality due to
a) High input impedance b) high CMRR
c) Low output impedance **d) high open loop gain**
3. The most important element in the precision rectifier, apart from op-amp is
a) Feedback resistor **b) diode**
c) input resistor divider d) feedback capacitor
4. The important requirement of the additional component as in question (3) above, is that the element is assumed to have
a) Ideal behavior b) linear operation
c) Non-linear operation d) piece-wise linear operation
5. To minimize the response time and to improve the operating frequency requires the use of
a) Diode **b) two diodes**
c) Diode with battery in series d) diode with battery in shunt

Equipment required:

Equipment	Range/Type	Purpose
Dual regulated Power supply	$\pm 12V$	For biasing the device
Function generator	1 MHz	To provide input
Oscilloscope	20 MHz dual channel	To observe and measure input/output

Components of the circuit and their purpose:

Component	Specification	Quantity	Purpose
Op-amp	IC741	1	Amplification
Diode	1N4007	2	Rectification
Resistor R4	1 k Ω	1	Load

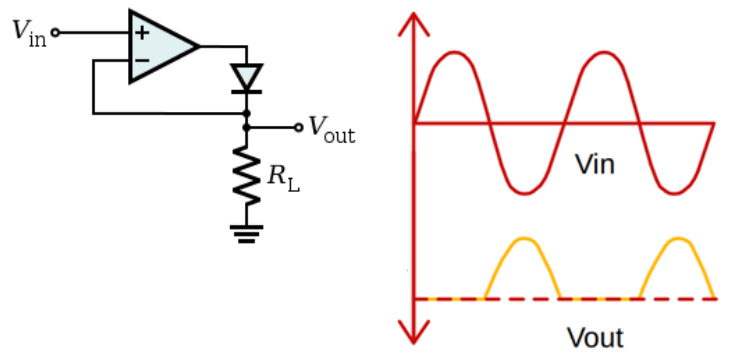
Theory:

- Precision rectifiers are circuits that rectify voltages below the level of cut-in voltage of the diode.
- The circuit uses op-amp in inverting mode and diode in the feedback path.
- It is used in Half wave rectifiers, Full wave rectifiers, peak value detector, clippers and clampers.

Procedure:

1. Construct the circuit as shown in figure
2. Set the function generator in sine wave mode and apply 100mV peak-to-peak, 1KHz signal to the input and observe the waveform using oscilloscope.
3. Observe the amplifier output waveform using oscilloscope.

Circuit Diagram



Understanding:

- The circuit rectifies signal below the cut-in voltage of diode.
- The circuit operates in first quadrant with $V_o > 0$.
- Negative output can be obtained by connecting diode in reverse direction.

Post – lab Questions:

1. Precision rectifiers are used in the following configuration(s)
a) Halfwave rectifier b) full waverectifier
c) Peakvalue detector d) **all of theabove**
2. Precision rectifiers are called so because rectifying voltages are _____ of the diode.
a) $>V_{cut-in}$ b) **$<V_{cut-in}$** c) $>V_F$ d) $<V_{BD}$
3. The diode used in the precision rectifier circuit is connected
a) At the input b) series with output
c) **In thefeedbackpath** d) in shunt with output
4. Precision rectifiers could also be used in
a) **Clipper circuits** b) resonance circuits c) voltage doubler d) zero voltage detector
5. To obtain negative polarity at the output
a) Input voltage polarity is reversed b) **diode connection is reversed**
c) a capacitor is used in feedback path d) capacitive load is used

Inverting and Non-inverting Comparator

Pre – Requisites:

The student should have completed the following study before doing this experiment

- Ideal characteristics of an op-amp
- Open-loop configuration of op-amp

Pre – lab Questions:

1. The op-amp in voltage comparator operates in _____ mode.
a) Inverting b) non-inverting c) **differential** d) summing
2. The op-amp employed in voltage comparator is in _____ configuration.
a) Positive feedback b) negative feedback c) **open-loop** d) closed loop
3. If the bias voltage to the op-amp is $\pm 20V$, the output swings between
a) **+20V and -20V** b) 0V and -20V
c) +12V and -12V d) 0V and +20

4. The output voltage is normally clamped using
 a) Voltage divider b) feedback resistor **c) diodes**
 d) zener diodes
5. The speed of operation of the comparator depends on
 a) Clamping diodes b) gain of op-amp
 c) clamping zener diode d) power supply

Equipment required

Equipment	Range/Type	Purpose
Dual Regulated Power supply	$\pm 12\text{VDC}$	For biasing the device
Regulated power supply	(0 – 12V) DC	Reference voltage
Oscilloscope	20 MHz Dual channel	To observe and measure input and output

Components of the circuit and their purpose

Component	Specification	Quantity	Purpose
Op-amp	IC741	1	Switching
Resistor R1	10k Ω	1	Current limiting
Resistor R2	10k Ω	1	Load resistor

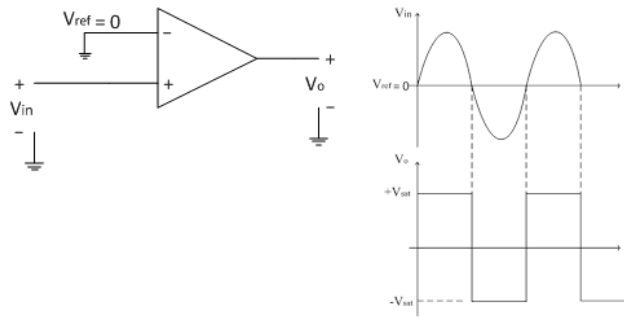
Theory:

- Voltage comparator is a circuit which compares unknown signal voltage with a known reference voltage.
- Voltage comparator consists of an op-amp operated in open-loop with signal voltage applied at one input and known reference voltage at the other input.
- A fixed reference voltage V_{ref} is applied to the inverting terminal and a time varying signal is applied to the non-inverting terminal of the op-amp.
- Op-amp, in open-loop, produces one of the two saturation voltages $\pm V_{sat}$ at the output.
- When V_{ref} is positive, the circuit acts as positive comparator and when V_{ref} is negative, the circuit acts as negative comparator.

Procedure:

1. Construct the circuit as shown below in figure
 2. Set the voltage in V1 to 7V
 3. Set the reference voltage V2 to +6V.
 4. Observe simultaneously the input and output waveform using oscilloscope.
- Repeat the above steps by changing the reference voltage V2 to -2V.

Circuit Diagram:



Understanding:

- In voltage comparator, op-amp operates in open-loop configuration.
- When $V_i < V_{ref}$, the output is at $-V_{sat}$.
- When $V_i > V_{ref}$, the output is at $+V_{sat}$.
- By interchanging input and reference voltages, the voltage comparator circuit can be modified as an inverting comparator.
- When $V_{ref} = 0$, the circuit becomes a zero crossing detector.

Zero Crossing Detector

Prerequisites:

The student should have completed the following study before doing this experiment

- Ideal characteristics of an op-amp
- Open-loop configuration of op-amp

Pre Lab Test:

1. In zero crossing detector circuit, the op-amp is used as
 a) Inverting amplifier b) non-inverting amplifier **c) comparator** d) Schmitt trigger

2. A zero crossing detector has a bias voltage of $\pm 10V$. When input voltage is positive, the output voltage is
 a) +10V b) 0V **c) -10V** d) +20V

3. In general terms, when the input voltage is negative, the output voltage is
 a) Equal to input voltage b) zero
c) Equal to positive bias voltage d) equal to negative bias voltage

4. In a zero crossing detector circuit, the non-inverting input terminal of the op-amp is
 a) Connected to the input signal **b) grounded**
 c) Connected to feedback circuit d) left open

5. The zero crossing detector circuit is similar in operation to
 a) Voltage follower b) integrator
c) Schmit trigger d) monostable multivibrator

6. The reference voltage for the zero crossing detector is kept at
 a) +Vcc b) -V_{EE} **c) 0V** d) -Vcc

Equipment required:

Equipment	Range/Type	Purpose
Dual Regulated Power supply	$\pm 12VDC$	For biasing the device
Oscilloscope	20 MHz Dual channel	To observe and measure input and output

Components required and their purpose:

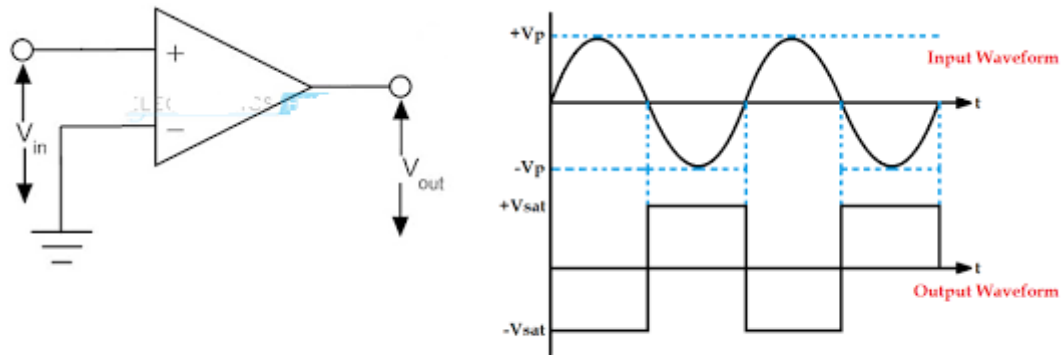
Component	Specification	Quantity	Purpose
Op-amp	IC741	1	Switching
Resistor R1	1k Ω	1	Current limiting
Resistor R2	1k Ω	1	Load resistor

Theory:

- Zero crossing detectors is a sine wave to square wave converter.
- Zero crossing detector circuit is a comparator with zero reference voltage.
- When the input signal voltage passes through zero in the negative and the positive directions, the output waveform switches between positive and negative saturation levels respectively.

Procedure:

1. Construct the circuit as shown below in figure
 2. Set the Function Generator in sinusoidal mode at 1 kHz and adjust the amplitude to 6 V peak to peak .
 3. Observe simultaneously the input and output waveform using oscilloscope.
- Repeat the above steps by interchanging the reference voltage and input signal.



Understanding:

- Zero crossing detector circuit is simply a modified version of voltage comparator with reference voltage as zero.
- In zero crossing detectors, op-amp operates in open-loop configuration.
- When the input voltage crosses zero, the output switches between $+V_{sat}$ and $-V_{sat}$.
- Clamping diodes at the input protects the op-amp from damage due to excessive voltage.
- By interchanging input and reference voltages, the circuit can be modified as a non-inverting zero crossing detector

Post Lab Questions:

1. The zero crossing detector output could be controlled using a
 - a) Clamping pn junction diode
 - b) capacitor in feedback
 - c) Clamping zener diode
 - d) transistor**
2. If the frequency f of the sine wave input to the circuit is doubled, the output frequency is
 - a) $f/2$
 - b) $2f$**
 - c) $f/4$
 - d) $4f$
3. If a zero crossing detector has an input of amplitude 15 V and a power supply voltage of $\pm 10V$, the Maximum output voltage is
 - a) +15V
 - b) +25V
 - c) +10V**
 - d) +5V

4. If the power supply voltage to the zero crossing detector circuit is decreased from $\pm 10\text{V}$ to $\pm 8\text{V}$, the Minimum output voltage is

- a) 0V **b) -8V** c) -10V d) -18V

5. In zero crossing detector circuit, to protect the op-amp from excess voltage at the input,

_____ is/are

Used.

- a) A series capacitor b) a transistor c) a shunt capacitor **d) pn junction diodes**

6. The speed of operation of zero crossing detector is due to

- a) diode in the feedback path **b) regenerative feedback**
c) Zener diode in the feedback path d) a +ve reference supply

RESULT:

Thus, the use of op-amp as precision rectifier, voltage comparator and zero crossing detector was studied

2. FREQUENCY RESPONSE OF ACTIVE FILTER

Aim:

To obtain the response of active filters by varying the frequency.

(i) First Order Low Pass Filter

Pre Requisites:

The students should have completed the following study before doing the experiment.

- Non inverting opamp.
- Concept of virtual ground in non inverting amplifier.
- Concept of passive filters.

Pre – lab questions:

1. The desirable feature(s) of filters is/are
 - a) Sharp cut-off
 - b) Lesser pass band ripple
 - c) Good phase response
 - d) All of the above**
2. The Butterworth filter is characterized by
 - a) High gain
 - b) Lesser pass band ripple
 - c) Sharp cut-off
 - d) All the above
3. The circuit arrangement that provides optimal performance in active filter is
 - a) Butterworth
 - b) Chebyshev
 - c) Sallen-Key**
 - d) Bessel
4. An active filter uses
 - a) Diode
 - b) Op-amp**
 - c) Zener
 - d) SCR
5. A filter is a circuit that
 - a) Provides amplification
 - b) Removes noise
 - c) Is frequency selective**
 - d) Is an all-pass circuit
6. The cut off frequency of the low pass filter depends on
 - a) op-amp gain
 - b) feedback resistor
 - c) input resistor
 - d) RC network**

Equipment requirement:

Equipment	Range/Type	Purpose
Fixed Power supply	$\pm 12\text{V DC}$	To provide operating voltage
Function generator	1 MHz	To provide input signal
Oscilloscope	20 MHz Dual channel	To observe and measure input and output

Components required:

Component	Specification	Quantity	Purpose
Op-amp	IC741	1	Amplification
Resistor R1	Potentiometer	1	Current limiting
Resistor R2	10k	1	Load
Resistor R3	10k	1	Determines gain
Resistor R4	10k	1	Feedback
Capacitor	$0.01\mu\text{F}$	1	Filter element

Theory:

- A filter is a frequency selective circuit that allows only a certain band of frequency components of an input signal to pass through and blocks other frequency components.
- An active filter network is obtained by interconnecting passive elements and active element.
- Op-amp used in active filter also provides amplification.

- A low-pass filter allows only low frequency signals and suppresses high frequency signals.
- The range of frequency varies from dc to cut-off frequency f_L . The frequency range below cut-off frequency is called *passband* and frequency range beyond f_L is called *stopband*.
- The gain of the filter

$$\frac{V_o}{V_{in}} = \frac{A_f \left(\frac{f}{f_L} \right)}{\sqrt{1 + \left(\frac{f}{f_L} \right)^2}}$$

Formula:

$$\text{Gain, } \left| \frac{V_o}{V_{in}} \right| = \frac{A_F}{\sqrt{1 + \left(\frac{f}{f_H} \right)^2}}$$

$$\text{Phase angle, } \phi = -\tan^{-1} \left(\frac{f}{f_H} \right)$$

DESIGN:

Design of I order Butter worth filter:

Given the cut off frequency F_L , A_O ,

$$F_L = 1/2\pi RC$$

Assume C and then substituting the value in the above formula

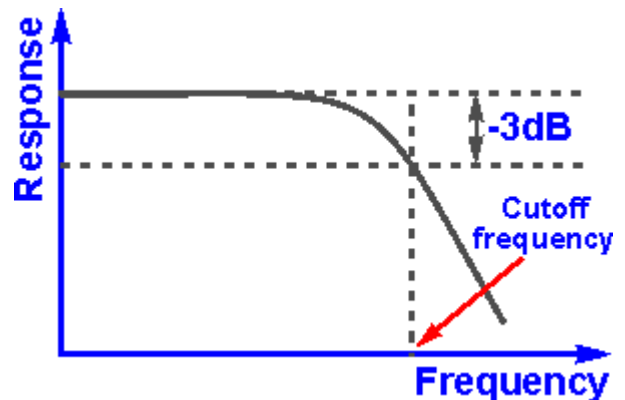
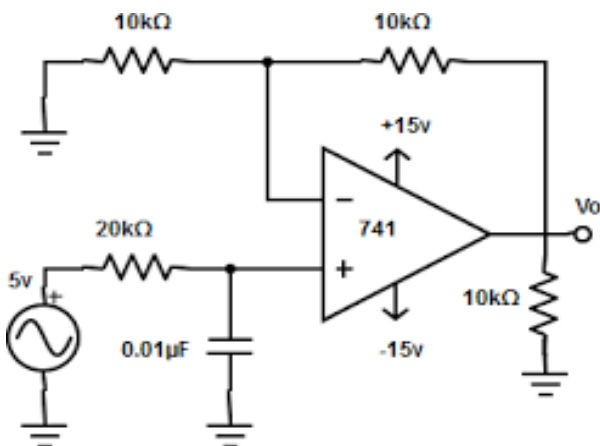
Find R, using A_O and assuming R1 find RF

Design of III order filter

As the third order filter is a combination of 1st order and 2nd order

Filter, the 2nd order can be designed in the same way as the 1st Order.

Circuit Diagram



Procedure:

1. Construct the circuit as shown above in figure
2. Set the Function Generator in sine wave mode and adjust the amplitude to 1 V_{peak-peak}.
3. Observe the waveform using oscilloscope.
4. Keeping the input voltage constant at 1V peak-peak, simulate the circuit for frequencies between 10 Hz to 100kHz.
5. Record the amplitude of output voltage for different input frequencies as per table.
6. Compute the gain for different frequencies.

Tabulation

Input voltage, $V_{in(PP)} = 1 \text{ V}$

Input frequency (Hz)	Output voltage, V_o (volts)	Gain = V_o/V_{in}	Gain(A) in dB = $20 \log_{10} V_o/V_{in}$
10			
20			
50			
100			
200			
500			
1k			
2k			
5k			
10k			
100k			

Understanding:

- Low pass filter allows low frequency signals and suppresses high frequency signals.
- At f_L the gain falls to $1/\sqrt{2}$ times the maximum gain.
- The frequency range from dc to f_L is called the passband.
- For $f > f_L$ (stop band) the gain decreases.
- Resistors R_3 and R_4 determine the gain of the filter.
- Gain is high at low frequencies.
- Rate of decay (roll-off rate) is low for first order filter.
- The *roll-off* rate improves with the order of the filter.

Post – lab Questions:

1. As the order of the filter increases,
a) **Sharpness at cutoff improves** b) gain increases
c) Stop band ripple reduces d) pass band ripples are absent
2. The cut-off frequency of the low pass filter is given by
a) $f=2\pi RC$ b) $f=2\pi/RC$
c) **$f= 1/2\pi RC$** d) $f =RC$
3. The cut-off frequency of a first order filter with $R = 1\text{ K}\Omega$ and $C = 0.5\ \mu\text{F}$ is
a) 500Hz **b) 330Hz**
c) 533Hz d) 300Hz
4. A first order filter with input resistor and feedback resistors of equal values, has Gain of
a) 1 b) 10
c) **2** d) 0.1
5. If the roll-over rate is -20 dB/decade, the addition of another order improves the Roll-over rate to
a) -10dB **b) -30dB**
c) -21 dB d) -40dB
6. To construct the second order low pass filter one of the following is required
a) A capacitor in the feedback path **b) another RC section**
c) Additional op-amp stage d) increase the op-amp gain

(ii) First and Third Order High Pass Filter

Pre Requisites:

The students should have completed the following study before doing the experiment.

1. Non inverting opamp.
2. Concept of virtual ground in non inverting amplifier.
3. Passive filter concept.

Pre lab Questions:

1. A high pass filter
 - a) Allows signals below cut off
 - b) Attenuates signals above cut off
 - c) Allows all signals
 - d) Allows signals above cut off**
2. The cut-off frequency of first order high pass filter using R and C is
 - a) RC
 - b) $1/RC$
 - c) $1/2\pi RC$**
 - d) $2\pi/RC$
3. The op-amp in the circuit provides
 - a) Filtering
 - b) Attenuation
 - c) Stability
 - d) Amplification**
4. The voltage gain of the active high pass filter is
 - a) $1+R_f$
 - b) $1+ R_f/R_i$**
 - c) R_f/R_i
 - d) $R_f.R_i$
5. The RC element is connected
 - a) At the inverting input
 - b) At the non-inverting input**
 - c) As feed back
 - d) In series with input resistance
6. The high pass filter could be converted to a low pass filter by
 - a) Removing the feedback
 - b) swapping R and C**
 - c) Reduce the gain
 - d) connect RC input to the inverting input

APPARATUS:

- 1) OP-AMP LM 741C-2
- 2) Resistors $10k\Omega$ -4, $16 K\Omega$ -3
- 3) Capacitors -0.01uf-3,
- 4) Function generator, TRPS, CRO, CRO Probes
- 5) Connecting wires, breadboard

Theory:

1. A filter is a frequency selective circuit that allows only a certain band of frequency components of an input signal to pass through and blocks other frequency components.
2. An active filter network is obtained by interconnecting passive elements and active element.
3. A high-pass filter allows only high frequency signals and suppresses low frequency signals.
4. The range of frequency beyond cut-off frequency, f_H is called *passband* and range of frequency from DC to f_H is called *stopband*.
5. The gain of the filter

DESIGN:

Design of I order Butter worth filter:

Given the cut off frequency F_L , A_O ,

$$F_L = 1/2\pi RC$$

Assume C and then substituting the value in the above formula

Find R, using A_O and assuming R1 find RF

Design of III order filter

As the third order filter is a combination of 1st order and 2nd order

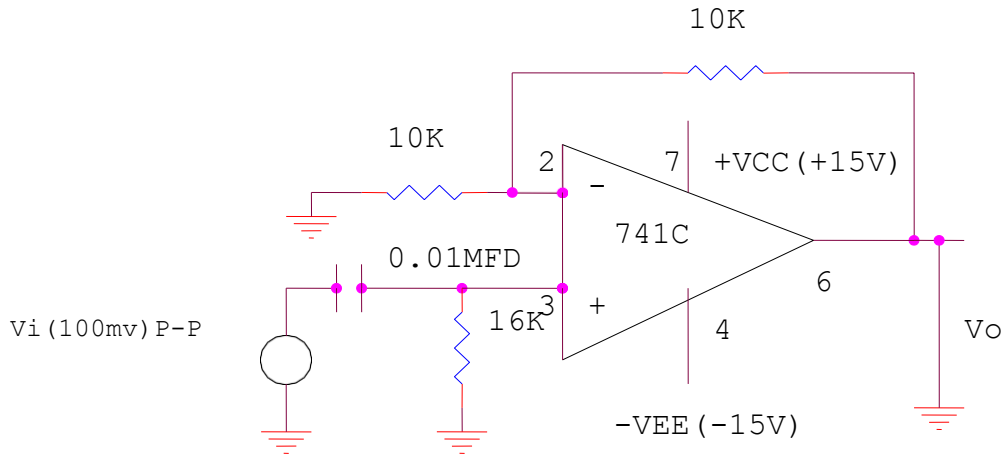
Filter, the 2nd order can be designed in the same way as the 1st Order

Procedure:

1. Construct the circuit as shown below in figure_
2. Set the Function Generator in sinusoidal mode and adjust the amplitude to $1V_{PP}$.
3. Observe the waveform using oscilloscope.

4. Keeping the input voltage constant at $1V_{PP}$, simulate the circuit for frequencies between 10 Hz to 100kHz.
5. Record the amplitude of output voltage for different input frequencies as per tabulation.
6. Compute the gain for different frequencies.

1st ORDER HIGHPASSBUTTERWORTH FILTER - Circuitdiagram



3 rd ORDER HIGH PASS BUTTERWORTH FILTER- Circuitdiagram

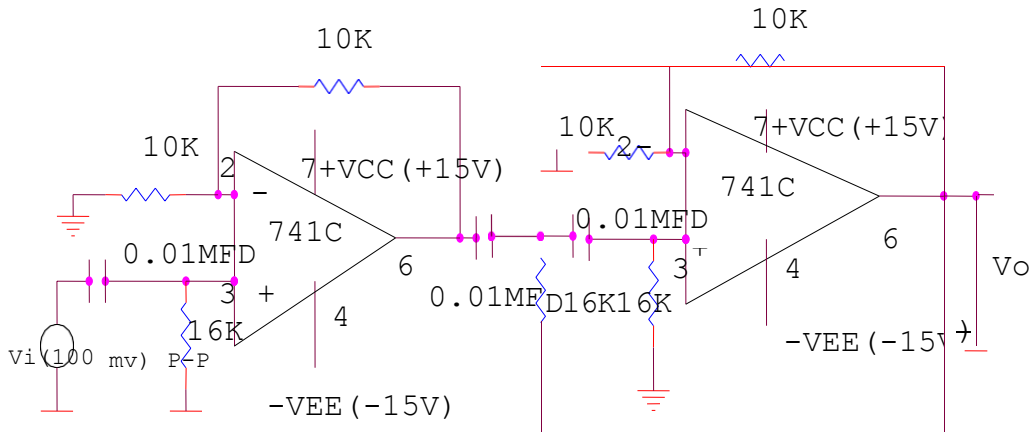
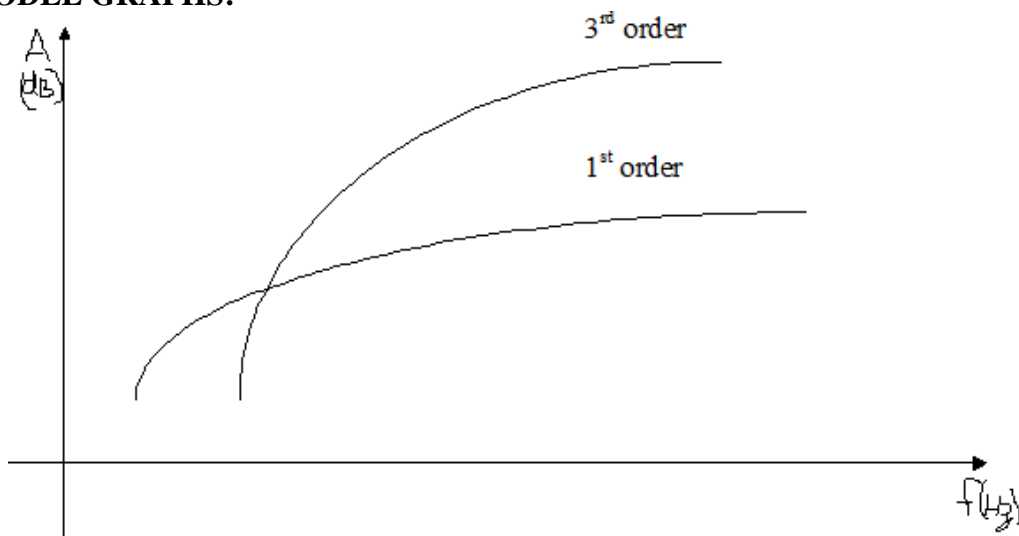


Table:

Input voltage, $V_{in(PP)} = 1\text{ V}$

Input frequency (Hz)	Output voltage, V_o (volts)	Gain $= V_o/V_{in}$	Gain(A) in dB $= 20 \log_{10} V_o/V_{in}$
10			
20			
50			
100			
200			
500			
1k			
2k			
5k			
10k			
100k			

MODEL GRAPHS:



Understanding:

- High pass filters allows high frequency signals and stop low frequency signals.
- The frequency range beyond f_H is called the passband.
- For $f < f_H$ (stop band) the gain is lower.
- Resistors R_3 and R_4 determine the gain of the filter.
- High pass filter is dual of low pass filter.
- Maximum gain occurs at high frequencies.
- At low frequencies gain is less.

Post – lab Questions:

1. A first order filter uses $R_f = 20 \text{ k}\Omega$ and $R_i = 10 \text{ k}\Omega$, the gain obtained is
a) 2
b) **3**
c) 1
d) 0.5
2. The cut-off frequency of the circuit using $R = 10 \text{ k}\Omega$ and $C = 0.01 \text{ }\mu\text{F}$ is
a) 159Hz
b) **159kHz**
c) 1.59MHz
d) 1.59kHz
3. The gain provided by the circuit using $R = 10 \text{ k}\Omega$ and $C = 0.01 \text{ }\mu\text{F}$ is
a) 10
b) 100
c) 159
d) **insufficient data**
4. In the second order high pass filter
a) **Another section of RC is used**
b) The positions of R and C is interchanged
c) An additional RC section is included at the feedback
d) An RC section is added to the input resistor
5. Addition of RC section in higher order filters
a) Increases ripple
b) Reduces ripple
c) **Improves cutoff**
d) Provides stability
6. The value of resistor in the RC network of the filter is doubled, the cut off frequency
a) Doubles
b) is not affected
c) **reduces by half**
d) reduces by 20%

RESULT:

The first order low pass and first and third order high pass filters were studied

3. SCHMITT TRIGGER

Aim:

To observe the output waveform of a Schmitt trigger circuit and to note down the hysteresis voltage V_{HY} with reference to upper and lower threshold voltages V_{UT} and V_{LT} respectively.

Pre-Requisites:

The student should have completed the following study before doing this experiment.

- Resistance divider network
- Op-amp characteristics
- Op-amp configurations

Pre-lab questions:

1. Schmitt trigger is an example of ----- circuit.
a) Amplifier b) oscillator **c) switching** d) power supply
2. In Schmitt trigger circuit, op-amp switches between
a) Cut-off and negative saturation **b) negative and positive saturation**
c) Slight conduction and cut-off d) cut-off and positive saturation
3. If the power supply voltage applied to the op-amp that has an open loop gain of 100dB is $\pm 20V$, the op-amp saturation voltage is
a) 20mV b) 2mV c) 20 μV d) 200 μV
4. The operation of a Schmitt trigger is similar to that of a
a) Full wave rectifier **b) series clipper** c) polarity detector d) clamper
5. The main application of Schmitt trigger is in
a) Amplifiers b) oscillators
c) **Sine wave to square wave converters** d) rectifiers
6. The speed of switching in the Schmitt trigger depends on
a) **Open loop gain** b) input resistor c) feedback resistor d) hysteresis

Equipment Required

Equipment	Range/Type	Purpose
Dual Regulated Power supply	(0 – 12V) DC	For biasing the device
Function generator	1 MHz	To provide input
Oscilloscope	20 MHz Dual channel	To observe and measure input/output

Components of the circuit and their purpose

Components	Specification	Quantity	Purpose
Op-amp	IC741	1	Amplification
Resistor R1	10k Ω	1	Input resistor
Resistor R2	2.2k Ω	1	feedback resistor
Resistor R3	2.2k Ω	1	feedback resistor

Theory:

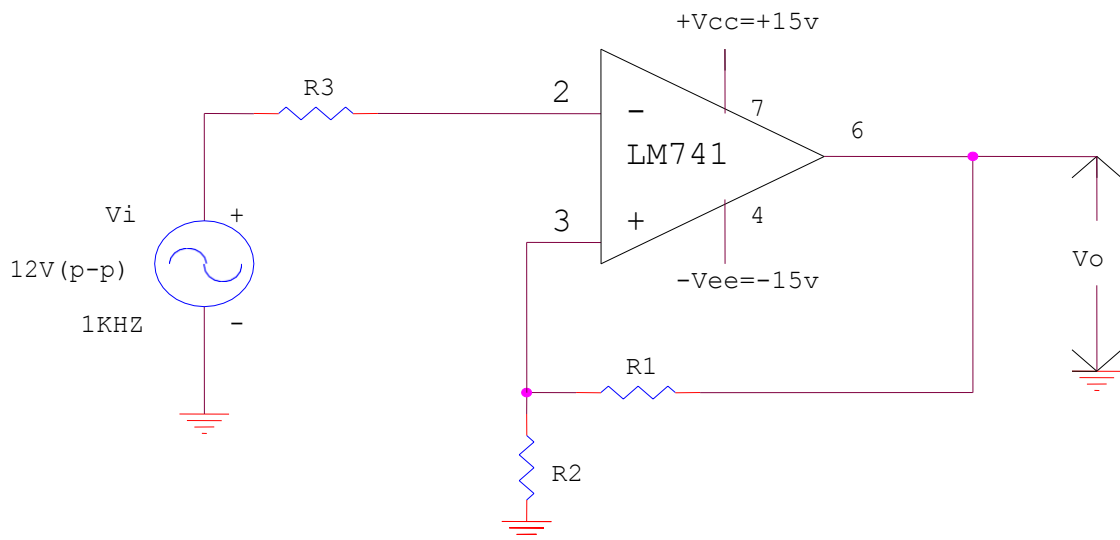
- Schmitt trigger is a comparator with positive feedback.
- It converts sine waveform into square wave.
- The input voltage triggers the output every time it exceeds threshold (upper threshold, V_{UT} and lower threshold, V_{LT}).
- The difference between the two voltage levels, V_{UT} and V_{LT} , is hysteresis voltage.
- The Schmitt trigger is also called regenerative comparator.

Procedure:

1. Construct the circuit as shown below
2. Set the Function Generator in sinusoidal mode and adjust the amplitude to 2 V peak to peak at 1kHz. Observe the waveform using oscilloscope.
3. Observe the output waveform using oscilloscope.

Circuit Diagram

Schmitt Trigger



$$R1=10K\Omega, R2 = R3 = 2.2K\Omega$$

Understanding:

- Schmitt trigger is a comparator with hysteresis.
- As it compares the input analog waveform with respect to preset values of V_{UT} and V_{LT} , Schmitt trigger is also known as two level comparator..
- A non-inverting Schmitt trigger circuit is obtained by interchanging V_i and V_{ref} .
- When an input sinusoidal signal of frequency f is applied, a square wave of same frequency is produced at the output.
- The square wave amplitude is symmetrical about zero level

Calculations:

Upper threshold voltage:

$$V_{UT} = \frac{R_2}{R_1 + R_2} (+V_{SAT})$$

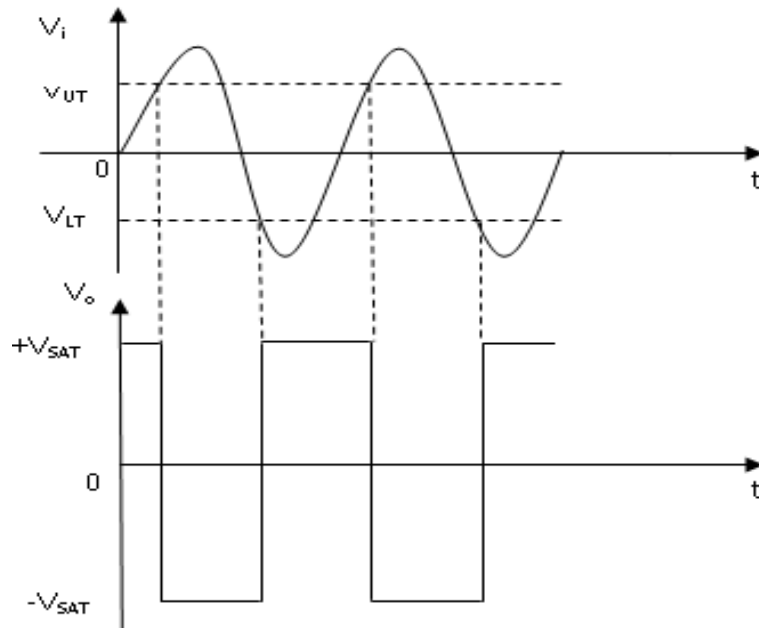
Lower threshold voltage:

$$V_{LT} = \frac{R_2}{R_1 + R_2} (-V_{SAT})$$

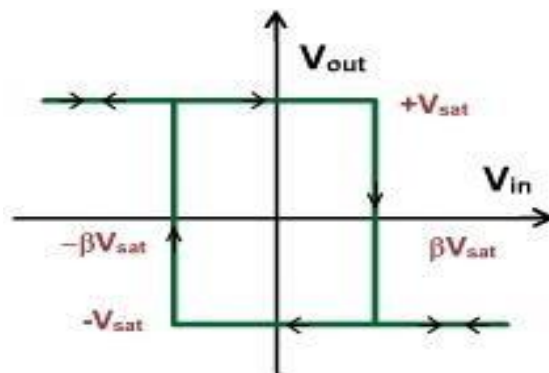
$$\text{Hysteresis voltage } V_{HY} = V_{UT} - V_{LT}$$

$$\text{Shift angle } \theta = \sin^{-1} (V_{UT}/V_p)$$

Input and output waveforms of Schmitt trigger:



V_o versus V_{in} plot or the hysteresis loop of Schmitt trigger:



Post – lab questions:

1. The speed of operation of Schmitt trigger depends on
 - a) op-amp gain
 - b) Rate of change of input**
 - c) Supply voltage
 - d) op-amp configuration

2. The switching speed could be improved by using
 - a) Zener diode at output
 - b) two Zener diode connected back to back at output**
 - c) Feedback resistor
 - d) capacitor in feedback

3. The Schmitt trigger could be used as
 - a) Voltage detector
 - b) astable multivibrator
 - c) Monostable multivibrator
 - d) **all of the above**

4. The feedback used in Schmitt trigger is
 - a) Degenerative
 - b) **regenerative**
 - c) Series
 - d) shunt

5. The value of cross over at increasing or decreasing input are called
 - a) Cut-off points
 - b) saturation points
 - c) **trip-point**
 - d) null points

6. The Schmitt trigger could also be used for
 - a) **Voltage level detection**
 - b) astable operation
 - c) Monostable operation
 - d) voltage limiting

RESULT:

Thus Schmitt trigger was designed and their operation was studied

4.(a) Design of Astable multivibrator using op amp

Aim:

To design and setup an astable multivibrator using opamp 741, plot the waveforms and measure the frequency of oscillation

Pre Requisites:

The student should have completed the following study before doing this experiment

1. Ideal characteristics of an op-amp.
2. Concept of inverting and non-inverting amplifiers
3. Theory of oscillators

Pre Lab Questions:

1. Astable multivibrator is an example of
 - a) Feedback circuit
 - b) Amplifier circuit
 - c) Regenerative switch**
 - d) bi-stable switch
2. The input voltage to astable multivibrator is derived through
 - a) Input applied to series resistor at the inverting input
 - b) Input applied to series resistor at the non-inverting input
 - c) Feedback obtained by voltage divider at the output
 - d) Feedback resistor between output and inverting input**
3. In astable multivibrator, the capacitor is connected
 - a) Between inverting input and ground**
 - b) Between non-inverting input and ground
 - c) Across feedback resistor
 - d) In series with feedback resistor
4. The capacitor C charges through the resistor R, towards
 - a) Input voltage
 - b) output voltage
 - c) Feedback voltage at output voltage divider**
 - d) ground voltage
5. Square wave output is obtained when 'ON' and 'OFF' times are
 - a) Maintained with the ratio 1:2
 - b) maintained with the ratio 2:1
 - c) Maintained with the ratio 1:1**
 - d) maintained with the ratio 1:4
6. During both 'ON' and 'OFF' states, the op-amp
 - a) Remains at cutoff
 - b) saturates
 - c) Swings between saturation and cutoff**
 - d) conducts slightly

Equipments required:

Equipment	Range/Type	Purpose
Dual Regulated Power supply	(0 – 12V) DC	For biasing the device
Oscilloscope	20 MHz Dual channel	To observe and measure input and output

Components required and their purpose:

Component	Specification	Quantity	Purpose
Op-amp	IC741	1	Amplification
Resistor R1, R2	10k Ω	2	Feedback Voltage divider
Resistor R3	4.7k Ω	1	Timing resistor
Capacitor, C1	0.1 μ F	1	Timing capacitor

Theory:

- Astable multivibrator is a rectangular wave generator. It is also called free running multivibrator.
- Astable multivibrator toggles between high and low states.
- There are no stable states in astable multivibrator.
- The reference voltage V_{ref} (βV_{sat} or $+\beta V_{sat}$) is applied to the non-inverting terminal.
- The resistors R_1 and R_2 form a voltage divider network and provide a fraction (β) of the output to the input as feedback.
- When input at the inverting terminal just exceeds V_{ref} switching takes place resulting in rectangular wave output.
- The duration the output remains high, is the time required for the capacitor to charge from $-\beta V_{sat}$ to $+\beta V_{sat}$.

Formula:

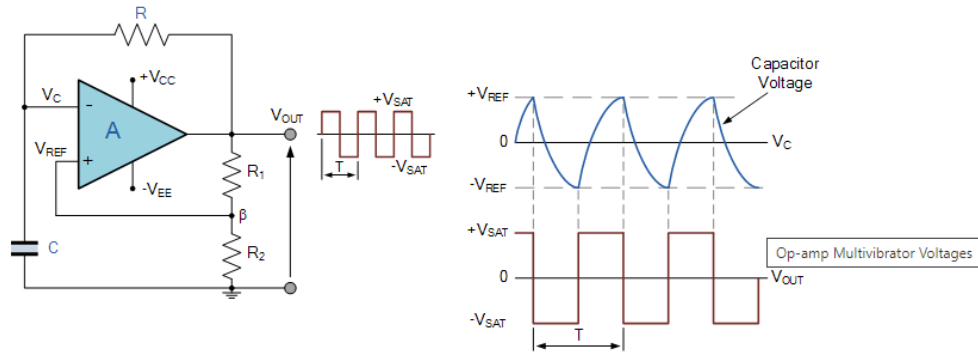
- $$T = 2RC \ln \frac{1 + \beta}{1 - \beta}$$

- $\beta = R_2 / (R_1 + R_2)$
- If $R_1 = 1.16 R_2, T = 2RC$

Procedure:

1. Construct the circuit as shown below in figure.
2. Observe simultaneously the output waveform and the voltage across the capacitor using oscilloscope.
3. Measure the amplitude and frequency.

Circuit Diagram:



$R_1 = R_2 = 10K\Omega, R = 4.7K\Omega, C = 0.1\mu F$

Understanding:

- When $V_o = +V_{sat}$ capacitor charges from $-\beta V_{sat}$ to $+\beta V_{sat}$ and switches the output V_o to $-V_{sat}$.
- When $V_o = -V_{sat}$ capacitor charges from $+\beta V_{sat}$ to $-\beta V_{sat}$ and switches the output V_o to $+V_{sat}$.
- In astable multivibrator, the op-amp operates in the saturation region.
- The output is fed back to the inverting terminal after integrating by a low pass RC combination.
- The duration T is set by external resistor and capacitor..
- The period of the output waveform can be changed by varying R3 or C1.
- The output amplitude can be varied by varying the power supply.

Post Lab Questions:

1. The 'mark' duration of the output is due to
 - a) **Capacitor charging time**
 - b) capacitor discharging time
 - c) Capacitor charging upto 1/3 of maximum
 - d) capacitor charging upto 2/3 of maximum

2. The 'space' duration of the output is due to the capacitor
 - a) Charging time
 - b) discharging time**
 - c) Discharging down to 1/3 of maximum
 - d) discharging down to 2/3 of maximum

3. The capacitor voltage during 'mark' is proportional to
 - a) $e^{-t/RC}$
 - b) $e^{t/RC}$
 - c) $e^{-t/RC}$**
 - d) $e^{t/RC}$

4. If feedback resistors used at the output are R_1 and R_2 , then the feedback factor, β is given by
 - a) $R_1 R_2 / R_1 + R_2$
 - b) $R_1 / R_1 + R_2$
 - c) $R_2 / R_1 + R_2$**
 - d) R_1 / R_2

5. If V_0 is the output voltage, then the feedback voltage is given by
 - a) $(R_1 R_2 / R_1 + R_2) V_0$
 - b) $(R_1 + R_2)$
 - V₀c) $(R_2 / R_1 + R_2)V_0$**
 - d) $(R_1 / R_1 + R_2)V_0$

6. The ON time of the astable multivibrator output is proportional to
 - a) Capacitor only
 - b) Resistor only
 - c) Both R and C**
 - d) input resistor R_i

4.(b)Design of Astablemultivibratorusing IC555

Aim:

To obtain a symmetric square wave output by maintaining certain duty cycle by using 555 timers

Pre – Requisites:

The student should have completed the following study before doing this experiment

- Functional blocks of 555 timer
- Concepts of capacitor charging and discharging
- Basics of voltage dividernetworks

Pre – lab Questions:

- 1) The astable multivibrator has_____stable states
 - a) One
 - b)Two
 - c)Zero
 - d) Complementary**
- 2) The main application of astable circuit is in
 - a) Gates
 - b)Adders
 - c)Clocks**
 - d) Memories
- 3) The astable circuit requires the following external components:
 - a) Capacitor and resistor**
 - b) Capacitors only
 - c) Capacitor and inductor
 - d) Inductor and resistor
- 4) When the duration of the ON and OFF states are equal, the output waveform is
 - a) Triangular
 - b)Rectangular
 - c)Sinusoidal
 - d) Square**
- 5) To achieve symmetry of the output waveform, the duration of two states of astable multivibrator should be in the ratio
 - a) 1: 2
 - b) 2:1
 - c) 1:1**
 - d) 1 : 3
6. The capacitor in the astable circuit charges towards V_{cc} through
 - a) R1 only
 - b)R2 only
 - c) R1and R2**
 - d) R1, R2 and ground
7. The capacitor discharges towards 0V,through
 - a) R1 only
 - b)R2 only**
 - c) R1andR2
 - d) R1, R2 and ground

Equipment required:

Equipment	Range/Type	Purpose
Dual Regulated Power supply	(0 – 12V) DC	Biassing the device
Oscilloscope	20 MHz Dual channel	To observe and measure input and output

Components Required:

Component	Specification	Quantity	Purpose
IC	555	1	Timer
Resistor R1, R2	47k Ω , 1k Ω	1	External timing
Resistor R4	220 Ω	1	Load
Capacitor, C1	10 μ F	1	External timing
Capacitor, C2	0.01 μ F	1	To bypass ripple

Theory:

- 555 timer is a device used for generating oscillation or introducing time delay.
- Astable multivibrator is a square wavegenerator
- Astable multivibrator toggles between one state and the other without the influence of any external control signal.
- It is also called free running multivibrator.
- The timing resistor is split into two sections, R1 and R2, the junction of which is connected to the discharge pin of 555timer.
- The interval during which the output remains high is the time required for the capacitor to charge from $(1/3) V_{CC}$ to $(2/3)V_{CC}$.
- The period is given by $T = 0.69 C(R_1+2R_2)$.

Formula:

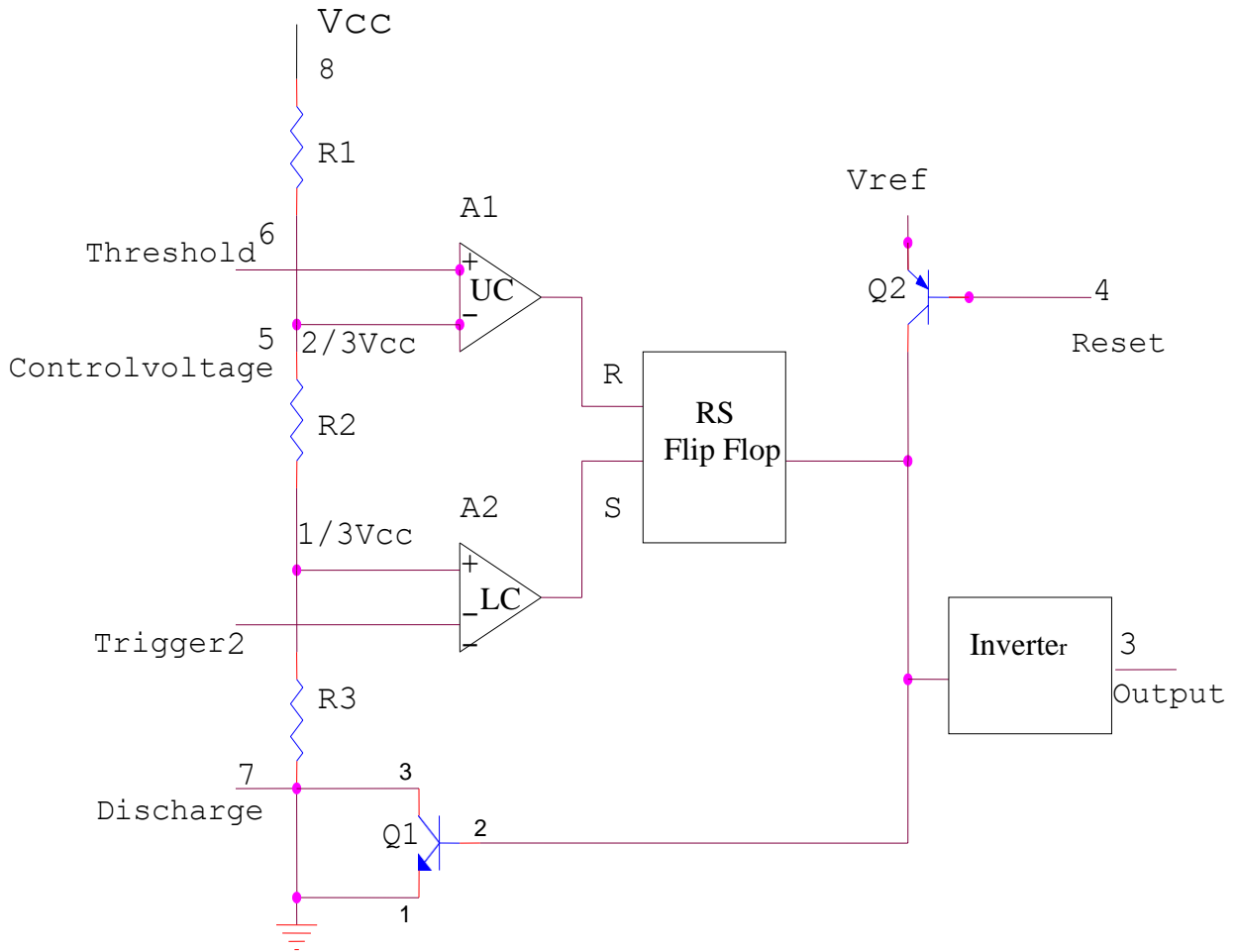
$$T_{ON} = 0.69 C (R_1 + R_2)$$

$$T_{OFF} = 0.69 C R_2$$

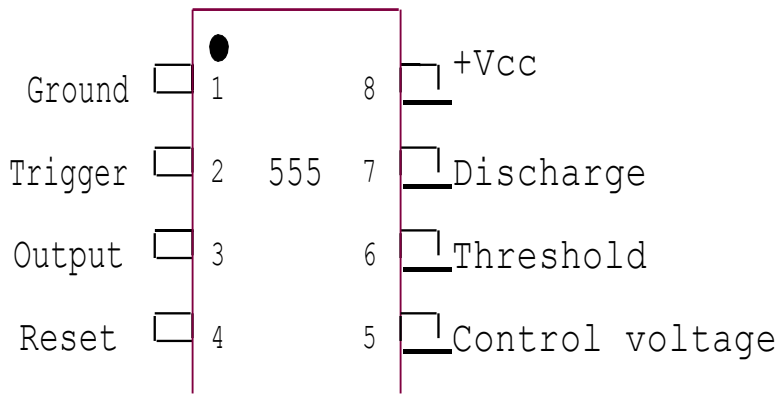
$$\text{Period, } T = T_{ON} + T_{OFF}$$

$$\text{Duty cycle} = 100 \times T_{ON} / (T_{ON} + T_{OFF})$$

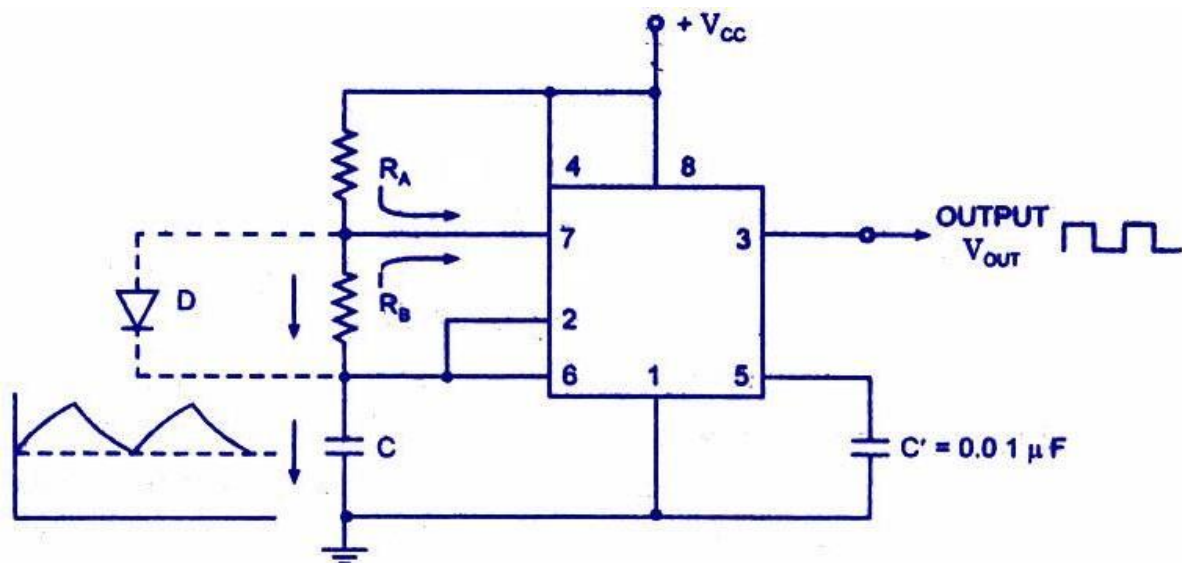
Internal block diagram of 555 IC



Pin Diagram



Circuit Diagram



Circuit of The Timer 555 as an Astable Multivibrator

$R_A=10K\Omega$ POT, $R_B=3.3K\Omega$, $C=0.1\mu F$, $V_{cc}=12v$

Procedure:

- Construct the circuit as shown above in figure.
- LED turns ON. After time T_{ON} , LED turns OFF.
- Observe simultaneously the output waveform and the voltage across the capacitor, C_1 , using oscilloscope.
- Measure the period (T_{ON} and T_{OFF}) of output waveform and calculate the duty cycle.
- Repeat the above steps by changing the values of R_2 and C_1 .

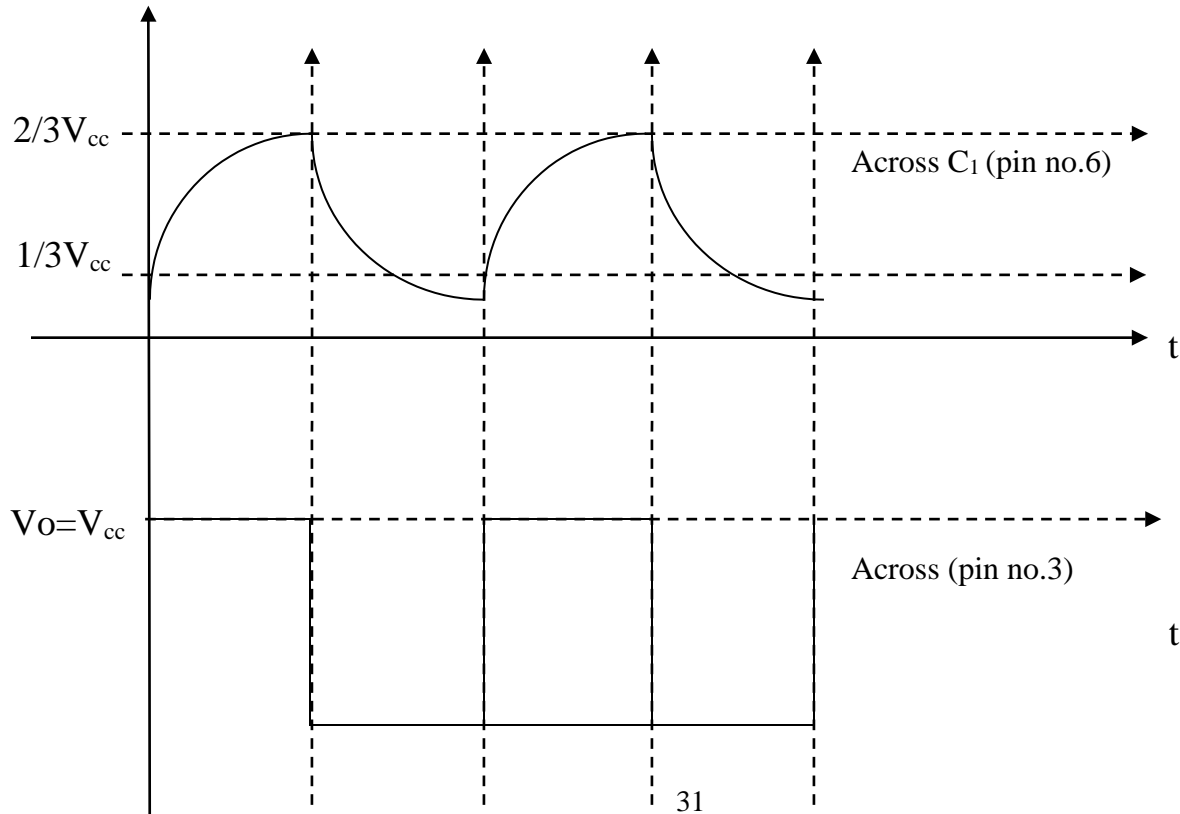
Tabulation:

S No	R_2	Theoretical Calculated frequency	Pulse T_{ON}	Pulse T_{OFF}	Period, $T_{ON} + T_{OFF}$	Frequency, $f (1/T)$	Duty cycle T_{ON}/T
1	1k Ω						
2	100 k Ω						
3	1 M Ω						

Understanding:

- When capacitor voltage, V_C , increases above $2/3 V_{CC}$, the output V_{out} is low and when it is below $1/3 V_{CC}$, the output V_{out} becomes V_{CC} .
- The waveform across capacitor shows charging and discharging through RC network.
- Astable multivibrator generates square wave.
- The duration, T , is determined by external resistor and capacitor.

MODEL GRAPHS:



Post – lab Questions:

- When the astable multivibrator is 'ON', the capacitor
 - Discharges**
 - Charges
 - Voltage remains same
 - Is open
- The capacitor charges towards V_{CC}
 - Directly
 - Through trigger input
 - Through resistors**
 - Through control terminal
- The charging time, in terms of the components is given by
 - $T = 0.69 (R_1 + R_2)$
 - $T = 0.69 (R_1 + R_2)C_1$**
 - $T = 1.1 (R_1 + R_2)$
 - $T = 1.1 (R_1 + R_2)C_1$
- The discharge time of capacitor in terms of the components is given by
 - $T = 1.1R_2C_1$
 - $T = 1.1 R_1 R_2C_1$
 - $T = 0.69 R_2C_1$**
 - $T = 0.69R_1R_2C_1$
- The frequency of oscillation of the output waveform is given by
 - $0.69 / (R_1 + 2R_2)C_1$
 - $1.44 / (R_1 + 2R_2)C_1$**
 - $0.69 / (R_1 + R_2)C_1$
 - $1.44 / (R_1 + R_2)C_1$
- A square wave output is obtained in the astable multivibrator with resistors R_1 and R_2 in the the Ratio
 - 1:1
 - 1:2
 - 2:1**
 - 1:3
- In a 555IC based astable multivibrator circuit if resistors $(R_A + 2R_B)$ and capacitor C are in the Ratio 1000:1, the frequency of oscillations is given by
 - 6.9kHz
 - 1.44 MHz
 - 1.44kHz**
 - 0.69 kHz

8. The duty cycle of a square wave in terms of TON and TOFF is in the ratio

a) $T_{ON} = 2T_{OFF}$

b) $T_{ON} = T_{OFF}$

c) $2T_{ON} = T_{OFF}$

d) $T_{ON} = 3T_{OFF}$

RESULT:

Thus the Astable multivibrator circuit using IC555 and Op-amp(LM 741) were constructed and verified its theoretical and practical time period

5. IC VOLTAGE REGULATOR

Aim:

To obtain the voltage regulation of a 3-terminal fixed IC voltage regulator.

Pre – Requisites:

The student should have completed the following study before doing this experiment

- Concepts of regulated power supply
- Zener diode as regulator

Pre – lab Questions:

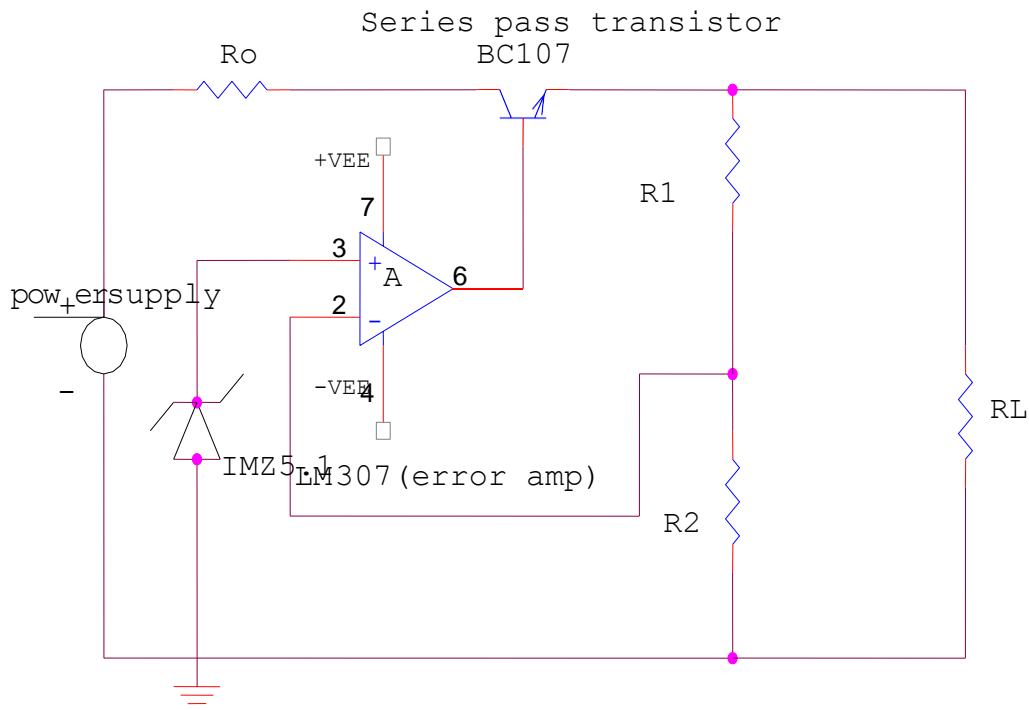
1. The voltage regulator provides constant dc voltage against variations in
a) Ripple b) load current c) input voltage **d) all of the above**
2. In the series regulator the most important component is the
a) Resistor b) capacitor c) diode **d) transistor**
3. The type of diode employed in voltage regulator circuit is usually
a) PN Junction diode **b) Zener diode**
c) Tunnel Diode d) PIN diode
4. When a series transistor is used in voltage regulator circuit, it is employed in
a) CE Configuration b) CB Configuration
c) CC Configuration d) any of the above configuration
5. The terminals of the transistor that are in series with the load (input – output) are
a) base-emitter b) base-collector
c) collector-emitter d) emitter-collector
6. A decrease in output voltage in the series voltage regulator leads to
a) Decrease in voltage across zener
b) Increase in voltage across base-emitter of transistor
c) Reduces transistor conduction
d) Comparator circuit being idle
7. An increase in output voltage is sensed by
a) **Sampling circuit** b) comparator circuit
c) Transistor collector-emitter circuit d) zener diode

Equipment required:

- 1) Ammeter (0-100)mA
- 2) Voltmeter (0-10)V
- 3) Capacitor $1\mu\text{F}$, $0.1\mu\text{F}$
- 4) Voltage regulator 7808
- 5) Decade resistance box(DRB)
- 6) TRPS
- 7) Breadboard
- 8) Connectingwires.

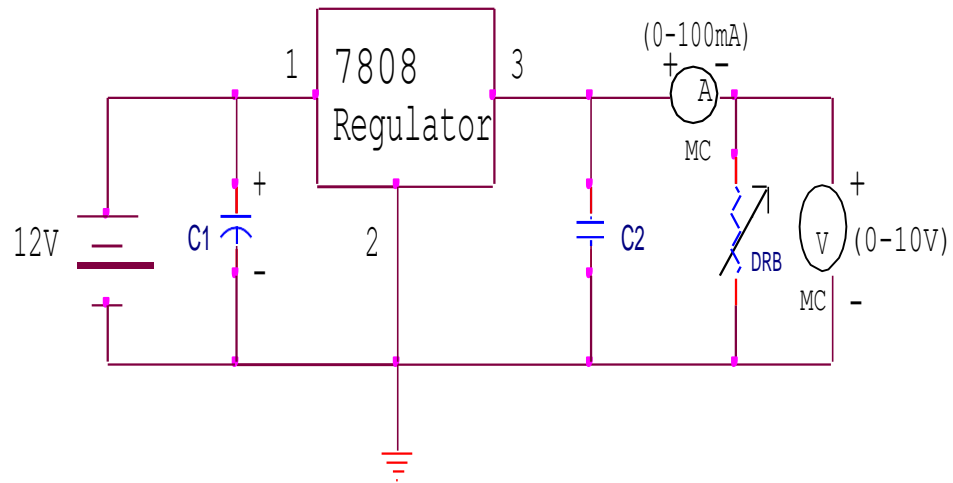
Theory:

- Voltage regulator is a circuit that maintains the output voltage of power supply constant against the variations of input voltage and changes of load current.
- Zener diode in reverse bias mode is employed as regulator.
- Zener voltage at breakdown region remains almost constant irrespective of the current through it.
- Transistor Q1 is a series pass element which functions as an emitter follower and Q2 functions as voltage comparator and dc amplifier.



Circuit Diagram:

3-Terminal Fixed Voltage Regulator



$C1 = 1\mu F, C2 = 0.1\mu F$

Tabular form:

Table1:

S.No	V_{in} (Volts)	V_{NL} (Volts)

Table1:

R_L (Ω)	I (mA)	V (Volts)	$V_{NL} =$ % Regulation

Procedure:

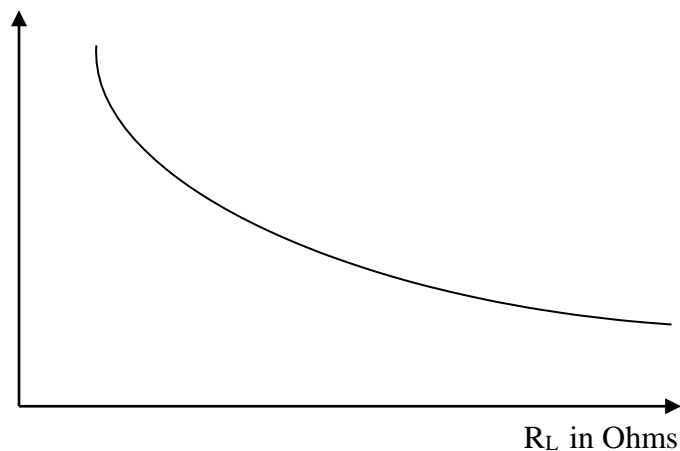
1. Connections are made as per the circuit diagram.
2. By adjusting the Voltage across RPS to 12V, the load terminals open circuited, the voltmeter reading is noted. This gives the no load voltage.
3. The load is varied from 10KΩ to 50Ω with the help of decade resistance box the corresponding voltmeter and ammeter reading are noted.
4. A graph is drawn between % voltage regulation on y-axis and load resistance on x-axis.
$$\% \text{ voltage Regulation} = \frac{V_{NL} - V_L}{V_L} \times 100$$

Understanding:

- Output voltage is constant irrespective of change in supply voltage and load current.
- Series regulators are used in high current and high voltage circuits, whereas shunt regulators are used in low voltage and low current circuits.

Model Graph:

% Regulation



Post – lab Questions:

1. The reference voltage required for the series regulator is provided by
 - a) **Zener diode**
 - b) comparator
 - c) Sampling circuit
 - d) transistor emitter
2. The feedback section of a series regulator consists of
 - a) Comparator
 - b) sampling circuit
 - c) Control circuit
 - d) **all of the above**

3. The current limiting in series voltage regulator is provided by using
 - a) **An additional transistor**
 - b) Op-Amp
 - c) voltage-divider resistor network
 - d) all of the above

4. The line and load regulation in series voltage regulator may be improved by using
 - a) An additional transistor
 - b) Op-Amp**
 - c) an additional zener diode
 - d) all of the above

5. The additional features that could be incorporated in a series regulator include
 - a) Current limiting circuit
 - b) foldback current limiting
 - c) Overvoltage protection
 - d) all of the above**

6. Assuming a Zener voltage of 12 V, if the applied input voltage to the series voltage regulator is 20V, the voltage across collector-emitter of the transistor is
 - a) 8V
 - b) 11.3V
 - c) 7.3V**
 - d) 11V

RESULT:

Thus the voltage regulation of a 3-terminal fixed IC voltage regulator was verified

6. Operation of R-2R ladder DAC and flash type ADC

Aim:

- To study the operation of
 i) R-2R DAC
 ii) Flash type ADC

APPARATUS REQUIRED:

S.NO	APPARATUS	RANGE	QUANTITY
1)	IC	$\mu A741$	1
2)	Resistor	1K Ω , 2K Ω	1
4)	Multimeter	-	1
5)	RPS	Dual Channel(0-30) V	1
6)	Connecting Wires		

Pre Lab Questions:

- The D-A (ladder network) converter requires
 - Resistor network only
 - Resistor network and active element only
 - Resistor network, active element and reference voltage**
 - Active element and reference voltage only
- The ratio of resistances in each section of the resistive network is
 - 1:1
 - 1:2**
 - 2:1
 - 1:10
- For a n-bit conversion, the number of resistor sections required are
 - n
 - 2n**
 - n/2
 - n²
- A 10-bit DAC provides voltage resolution between
 - Vref/ 2¹⁰**
 - Vrefx2¹⁰
 - Vrefx(2¹⁰-1)
 - Vref x2⁽¹⁰⁻¹⁾

THEORY:

In weighted resistor type DAC, op-amp is used to produce a weighted sum of digital inputs where weights are produced to weights of bit positions of inputs. Each input is amplified by a factor equal to ratio of feed back resistance to input resistance to which it is connected.

$$V_{OUT} = -R_F/R (D_3 + (1/2) D_2 + (1/4) D_1 + (1/8) D_0)$$

The R-2R ladder type DAC uses resistor of only two values R and 2R. The inputs to resistor network may be applied through digitally connected switches or from output pins of a counter. The analogue output will be maximum, when all inputs are of logic high.

$$V = -R_f/R \left(\frac{1}{2} D_3 + \frac{1}{4} D_2 + \frac{1}{8} D_1 + \frac{1}{16} D_0 \right)$$

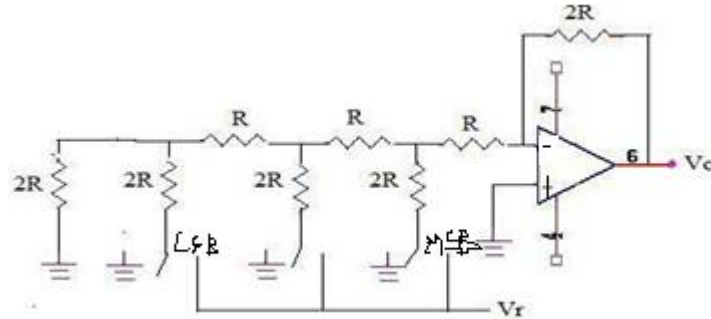
In a 3 input ADC, if the analog signal exceeds the reference signal, comparator turns on. If all comparators are off, analog input will be between 0 and V/4. If C1 is high and C2 is low input will be between V/4 and V/2. If C1 and C2 are high and C3 is low input will be between 3V/4 and V.

PROCEDURE:

1. Connect the circuit as shown in circuit diagram.
2. For various inputs, measure the outputs using multimeter.

CIRCUIT DIAGRAM:

a) R-2R Ladder DAC:

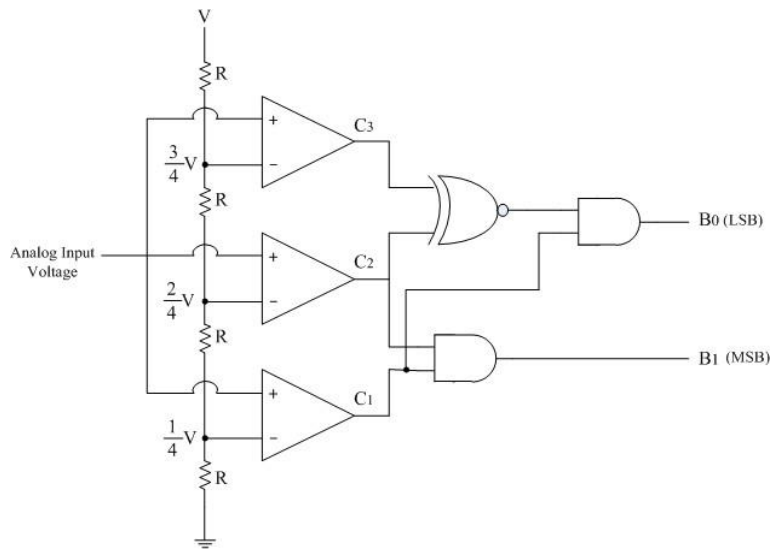


R=1KΩ

Input and Output Table:

S.No.	D2	D1	D0	Vth	Vprac
1)	0	0	0	0	0
2)	0	0	1	1.25	1.3
3)	0	1	0	2.5	2.7
4)	0	1	1	3.75	3.5
5)	1	0	0	5	4.9
6)	1	0	1	6.25	6.5
7)	1	1	0	7.5	7.2
8)	1	1	1	8.75	8.3

2 Bit Flash Type ADC



Input and Output Table:

Analog Input Conditions	Comparator Outputs			Digital output	
	C ₁	C ₂	C ₃	B ₁	B ₀
$0 \leq V_{in} \leq \frac{V}{4}$	0	0	0	0	0
$\frac{V}{4} \leq V_{in} \leq \frac{2V}{4}$	1	0	0	0	1
$\frac{2V}{4} \leq V_{in} \leq \frac{3V}{4}$	1	1	0	1	0
$\frac{3V}{4} \leq V_{in} \leq V$	1	1	1	1	1

Post Lab Questions (Part A)

1. **How many comparisons will be performed in an 8 bit successive approximation type ADC?**

8 Comparisons

2. **The basic step of 9 bit DAC is 10.3mV. If 00000000 represents 0V. What output is produced if the input is 101101111?**

7.38mV.

3. **State the applications of DAC and ADC.**

- a) Digital signal processing
- b) Communication circuits

4. **For R-2R ladder 4 bit type DAC find the output voltage if digital input is 1111. Assume $V_R = 10V$, $R = R_f = 10K$.**

$V_o = 9.375V$

5. **Which is the fastest type of ADC? Why?**

Successive approximation is the fastest type of ADC. It completes n-bit conversion in n clock periods.

Post Lab Questions: (Part b)

1. If the reference voltage is 10V in a 4-bit resistive network, the output voltage for digital input '1001' is

a) **5.625 V** b) 9 V c) 5 V d) 9.375V

2. If the reference voltage is 10V, the resolution of the 4-bit D-A converter is

a) 1 V b) 5 V c) **0.625V** d) 0.5V

3. A 10-bit DAC as above, uses 10V reference, the output voltage would be approximately in steps of

a) 1024mV b) **10mV** c) 100mV d) 1V

4. In the binary ladder circuit, the number of resistors required for n-bit realization is

a) nR b) 2nR c) (2nR)-1 d) **(2nR)+1**

5. The effective resistance, looking either backward or forward from any of the nodes in a binary ladder network is

- a) R **b)2R** c) R/2 d) 3R

6. If the input to a binary ladder circuit is '1000' and the reference voltage is 'V' volts, the output voltage is equal to

- a) V b)2V **c) V/2** d) 8V

7. An additional circuit that is required at each input node is

- a) Comparator **b)register** c)level amplifier d) ANDgate

RESULT:

The operation of R-2R ladder DAC and Flash type ADC was studied

8. Minimization and Realization of a given Function using Basic Gates(AND, OR, NOR, NAND,EXOR).

AIM:

- (i) To verify the truth tables of all logic gates.
- (ii) To Realize the Given Function Using Basic Gates
 $F(w, x, y, z) = \sum(0,1,2,3,4,5,6,9,10,11,12,13)$

APPARATUS:

- i) IC 74LS04 (NOTGate)
- ii) IC 74LS08 (two input ANDgate)
- iii) IC 74LS32 (two input ORgate)
- iv) IC 74LS86 (two input EX-ORgate)
- v) IC 74LS00 (two input NANDgate)
- vi) IC 74LS02 (two input NORgate)
- vii) Digital IC TrainerKit
- viii) Connecting Wires

Pre – lab Questions:

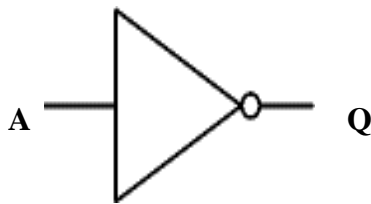
1. According to De Morgan's first Law, the complement of sum is equal to
 - a) '1'
 - b) **product of complements**
 - c) '0'
 - d) sum of complements
2. If three inputs A,B and C are used, then according to De Morgan's Law, $(A+B+C)'$ equals
 - a) $(A+B)'+C'$
 - b) $A+(B+C)'$
 - c) $A'B'C$
 - d) **$A'B'C'$**
3. When same inputs are applied to a 2-input NOR gate, the output obtained is
 - a) 1
 - b) **complement of input**
 - c) 0
 - d) same as input
4. The NOT function is performed using-----regions of transistor operation.
 - a) Active and cutoff
 - b) active and saturation
 - c) **Cutoff and saturation**
 - d) saturation
5. In a AND gate constructed using diodes, the input is applied to the _____ while the output is taken at the junction of _____.
 - a) anode,cathodes
 - b) **cathode, anodes**
 - c) either (a)or(b)
 - d) none of the above

6. The diode circuit in a OR-gate configuration

- a) Requires separate power supply
- b) Doesn't require power supply**
- c) Always has the diodes turned ON
- d) Always has the diodes turned OFF

NOT GATE:

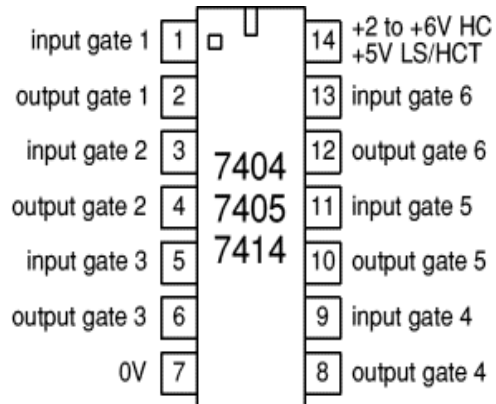
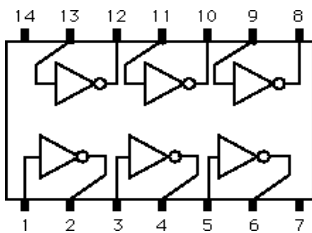
Symbol:



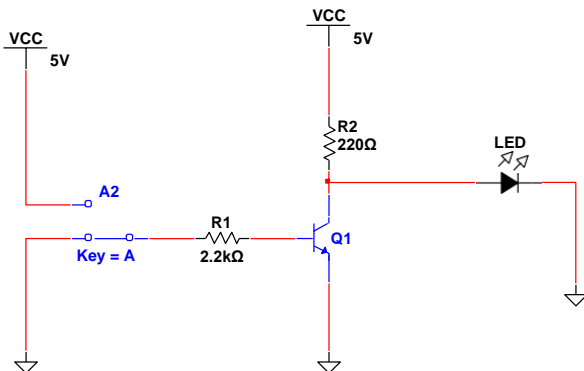
Truth table:

Input A	Output Q
0	1
1	0

PINDIAGRAM:

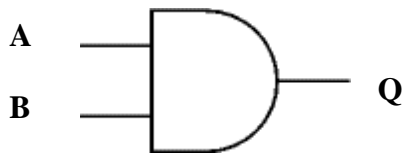


NOT Gate using Transistor

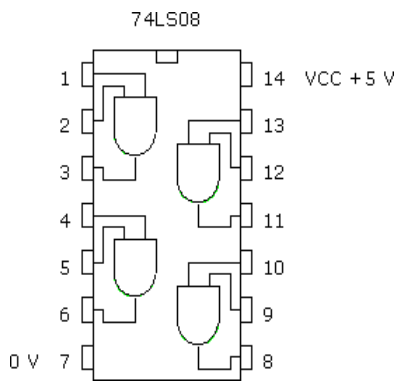


AND GATE:

SYMBOL:



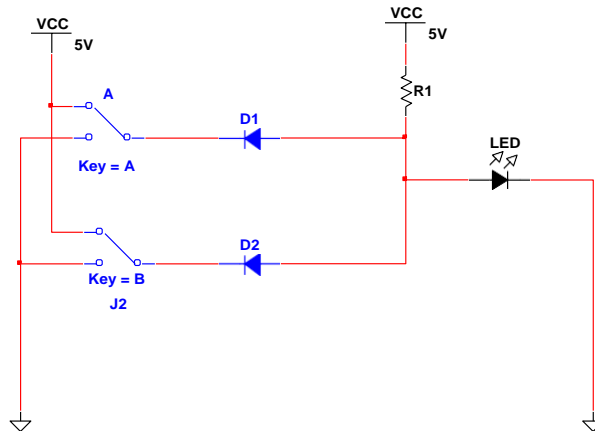
PIN DIAGRAM:



TRUTH TABLE:

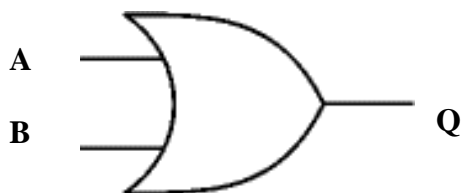
Input A	Input B	Output Q
0	0	0
0	1	0
1	0	0
1	1	1

AND gate using diodes

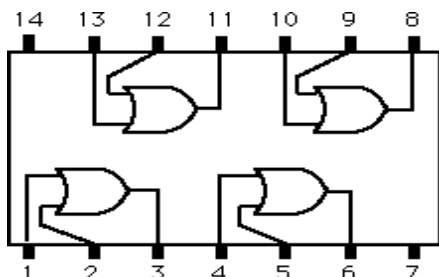


OR GATE:

SYMBOL:



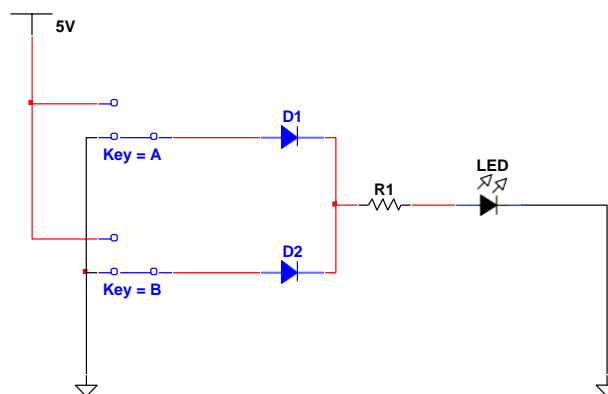
PIN DIAGRAM:



TRUTH TABLE:

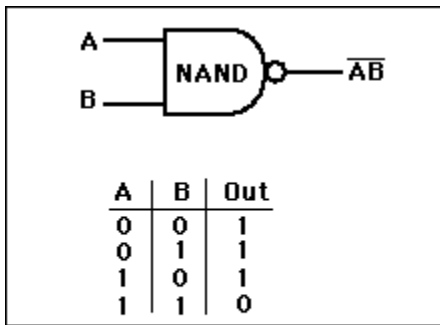
Input A	Input B	Output Q
0	0	0
0	1	1
1	0	1
1	1	1

OR Gates using Diodes

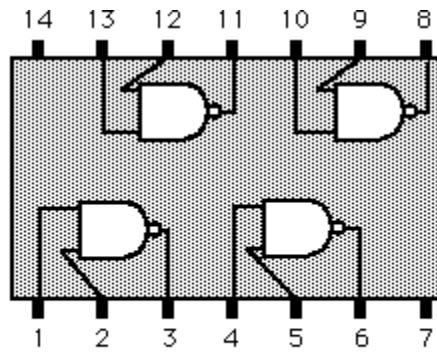


NAND GATE:

SYMBOL & TRUTH TABLE:



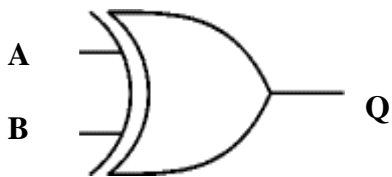
PIN DIAGRAM:



7400 or 74LS00 quad two-input NAND gate.

EXCLUSIVE -OR GATE:

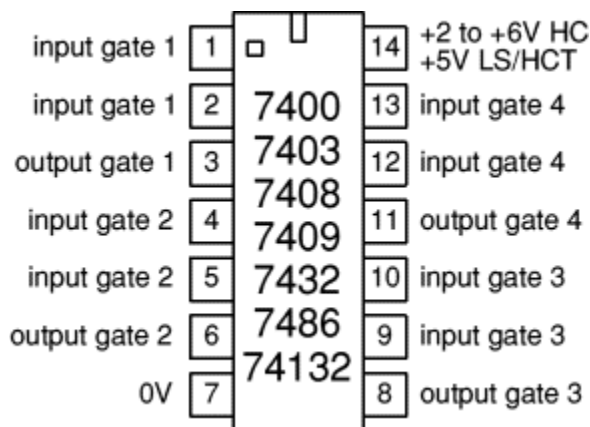
SYMBOL:



TRUTH TABLE:

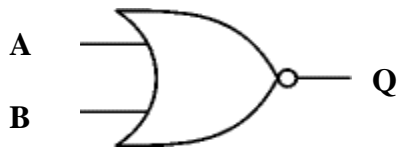
Input A	Input B	Output Q
0	0	0
0	1	1
1	0	1
1	1	0

PIN DIAGRAM:



NOR GATE

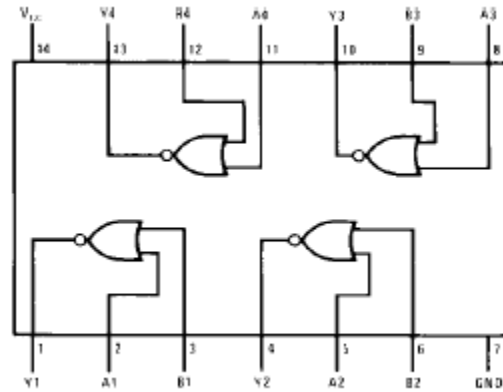
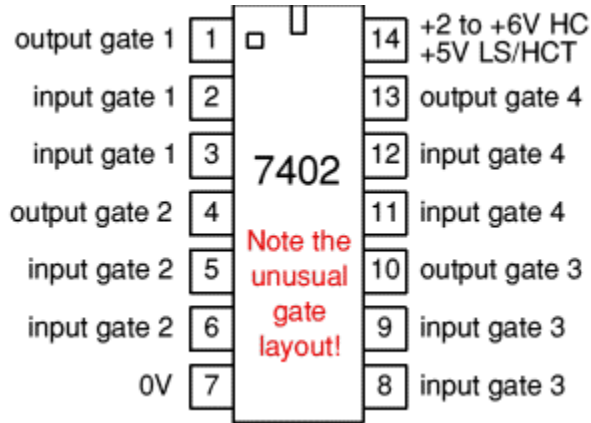
SYMBOL:



TRUTHTABLE

Input A	Input B	Output Q
0	0	1
0	1	0
1	0	0
1	1	0

PIN DIAGRAM:



MINIMIZATION

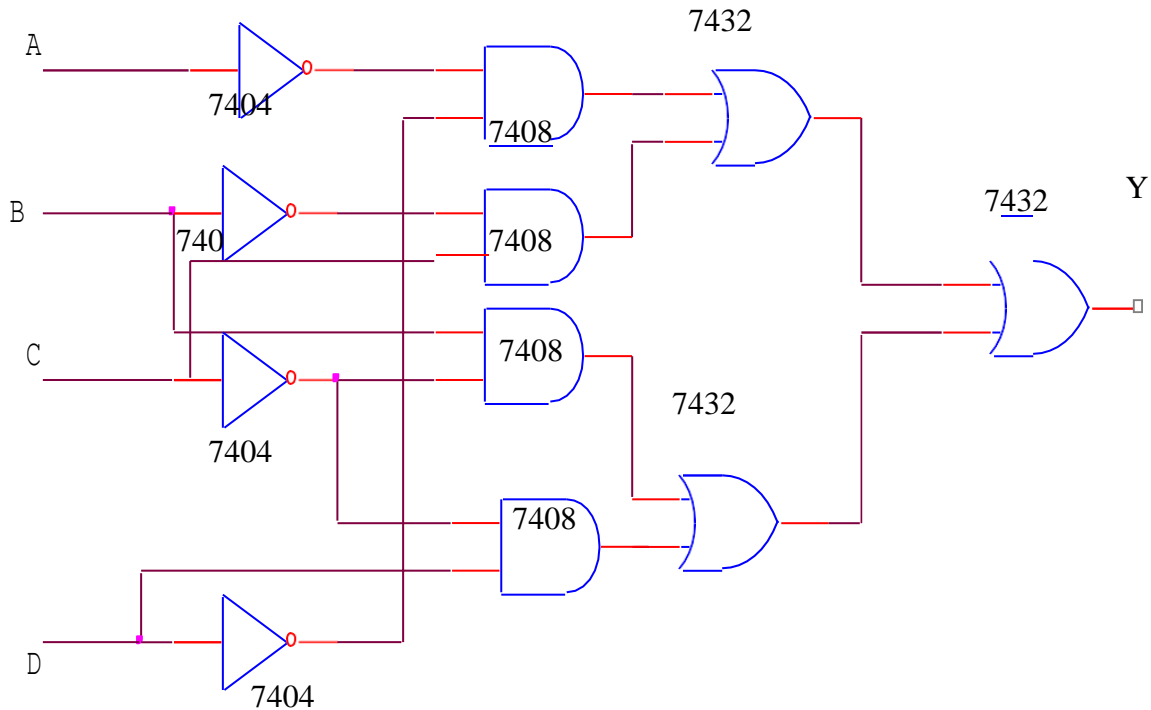
AB/CD	C'D'	C'D	CD	CD
A'B'	1	1	1	1
A'B	1	1	0	1
AB	1	1	0	0
AB'	0	1	1	1

$$Y = C^1D + C^1B + B^1C + A^1$$

D¹PROCEDURE:

1. The given function minimized using karnaugh maps.
2. Implement the logic diagram with truth table
3. Verify the Boolean function experimentally basic gates.
4. The truth tables are to be verified.

LOGIC CIRCUIT



Viva Questions:

1. What is SOP?

The logical sum of the several product variables is called sum of product. It is basically an OR operation of AND operated variables.

$$Y = AB + BC + CA$$

2. What is POS?

The logical product of the several sum variables is called product of sum. It is basically an AND operation of OR operated variables.

$$Y = (A+B)(B+C)(C+A)$$

3. State De Morgan's theorem?

The first theorem states that the complement of a product/sum is equal to the sum/product of the complements.

4. What is Minterm?

Product term containing all the possible variables of the function in either complement or uncomplimentary form is called Minterm.

5. What is Maxterm?

Sum term containing all the possible variables of the function in either complement or uncomplement form is called Maxterm

RESULT:

(i) The truth tables of six logic gates were verified

(ii) The given functions were realized using basic logic gates and the values of the truth table were verified.

9. Design and implementation of code converters using logic gates

(i) BCD to excess-3 code

Aim:

To construct the circuit of BCD to excess-3 code and Gray to Binary and study their working

Pre-lab questions:

- 1) BCD stands for
 - a. Binary code
 - b. Binary coded digit
 - c. Binary coded decimal
 - d. Binary coded display
- 2) Excess- 3 code of a given word is obtained by adding ----- to it
 - a. 3bits
 - b. Equivalent of decimal 3
 - c. '111'
 - d. '1'
- 3) The maximum value of each BCD digit is
 - a. 9
 - b. F
 - c. C
 - d. A
- 4) Each digit of decimal number in BCD is represented using
 - a. 1 bit
 - b. 2bits
 - c. 4 bits
 - d. 8 bits
- 5) the main applications of BCD is in
 - a. Memory circuits
 - b. Counters
 - c. calculators
 - d. Code

Components of the circuit and their purpose:

Component	Specification	Quantity	Purpose
NOT gate	74LS04 / 74HCT04	1	Combinational circuit element
2 input AND gate	74LS08 / 74HCT08	1	Combinational circuit element
2 input OR gate	74LS32 / 74HCT32	1	Combinational circuit element
2 input XOR gate	74LS86	1	Combinational circuit element
Digital IC trainer kit		1	Construct the circuit in simple way

Theory:

- A Code converter is a circuit that makes the two systems compatible, when uses a different binary code.
- BCD to Excess 3 code requires four input variables and four output variables since each code requires four bits to represent a decimal digit.
- The conversion logic is expressed

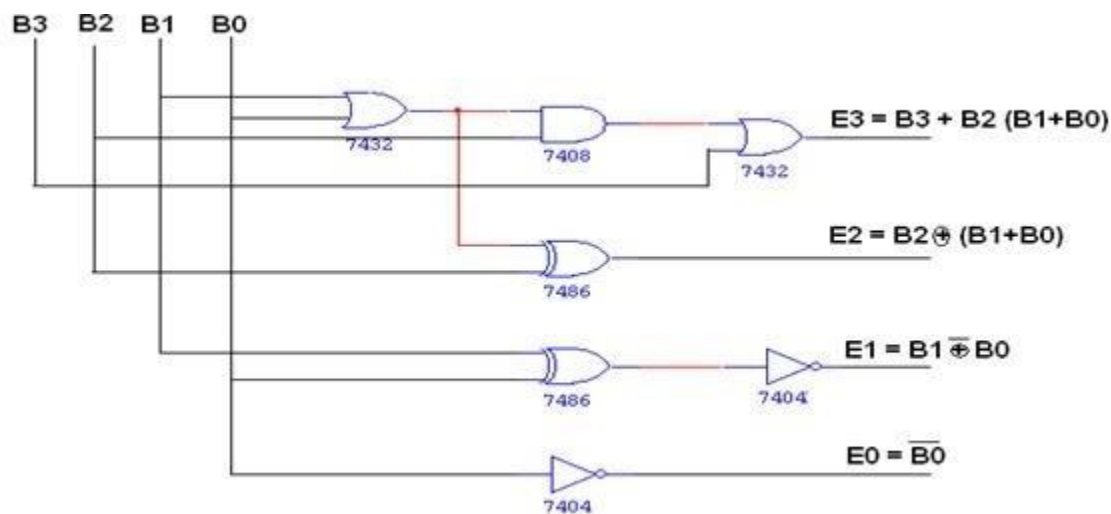
$$\text{as: } E_0 = B_0'$$

$$E_1 = B_0 B_1 + B_0' B_1'$$

$$E_2 = B_2 \text{ XOR } (B_1 + B_0)$$

$$E_3 = B_3 + B_2 (B_1 + B_0)$$

BCD to excess-3 code conversion



Procedure:

- Construct the circuit as shown in figure
- Select the switches A, B, C and D to provide input bit combinations.
- Observe the output LED for each input bit combinations and verify the truth table.

Truth Table:

BCD code input				XS3 code output			
B3	B2	B1	B0	E ₃	E ₂	E ₁	E ₀
0	0	0	0	0	0	1	1
0	0	0	1	0	1	0	0
0	0	1	0	0	1	0	1
0	0	1	1	0	1	1	0
0	1	0	0	0	1	1	1
0	1	0	1	1	0	0	0
0	1	1	0	1	0	0	1
0	1	1	1	1	0	1	0
1	0	0	0	1	0	1	1
1	0	0	1	1	1	0	0

Post-lab Questions:

- To convert an excess- 3 word to BCD
 - '111' is added
 - '011' is added
 - '011' is subtracted
 - '111' is subtracted
- The range of bits used for representing each BCD digit is
 - '0000' to '1111'
 - '0000' to 1001'
 - '0011' to 1001'
 - '0011' to '1100'
- BCD is an example of
 - 8421 code
 - weighted code
 - Reflex code
 - non-reflex
- The main advantage of BCD code is in
 - BCD additions
 - decimal subtractions
 - binary subtractions
 - binary addition
- The range of binary patterns disallowed for BCD is
 - '0000'to '0011
 - '1100'to '1111'
 - both (a) and(b)
 - Only (b)

(ii) Gray to binary

Aim:

To construct the circuit of BCD to excess-3 code and Gray to Binary and study their working

Pre-lab questions:

1. A code that uses one bit variations between successive code is
 - a. binary
 - b. gray
 - c. BCD
 - d. Excess-3
2. The logic operations used for binary to gray code conversion is
 - a. AND
 - b. NAND
 - c. EX-OR
 - d. NOR
3. The logic operations used for gray to Binary code conversion is
 - a. AND
 - b. NAND
 - c. EX-OR
 - d. NOR
4. The main application of gray code is in
 - a. decoders
 - b. arithmetic circuits
 - c. encoders
 - d. Multiplexers
5. The gray code cannot be used in
 - a. decoders
 - b. arithmetic circuits
 - c. encoders
 - d. Multiplexers

Components of the circuit and their purpose:

Component	Specification	Quantity	Purpose
2 input XOR gate	74LS86 / 74HCT86	1	Logic element
Digital IC trainer kit		1	Construct the circuit in simple way

Theory:

- A Code converter is a circuit that makes the two systems compatible, when uses a different binary code.
- In binary code, each decimal digit, 0 through 9, is coded by a 4-bit binary number.

- Gray code is a non-weighted code. It is a cyclic code as successive code words differ in one bit position only.
- The conversion logic is expressed as:

$$\mathbf{B_0 = G_0 \oplus G_1 \oplus G_2 \oplus G_3}$$

$$\mathbf{B_1 = G_1 \oplus G_2 \oplus G_3}$$

$$\mathbf{B_2 = G_2 \oplus G_3}$$

$$\mathbf{B_3 = G_3}$$

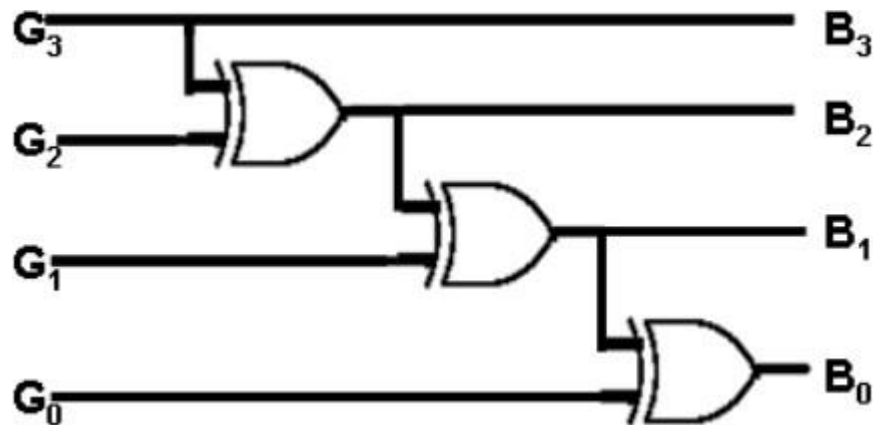
Procedure:

- Construct the circuit as shown in figure__using *spice* tool.
- Select the switches A, B, C and D to provide input bit combinations.
- Observe the output LED for each input bit combinations and verify the truthtable.

Truth Table:

4 bit Gray Code				4 bit Binary Code			
A	B	C	D	B ₄	B ₃	B ₂	B ₁
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	1	0	0	1	0
0	0	1	0	0	0	1	1
0	1	1	0	0	1	0	0
0	1	1	1	0	1	0	1
0	1	0	1	0	1	1	0
0	1	0	0	0	1	1	1
1	1	0	0	1	0	0	0
1	1	0	1	1	0	0	1
1	1	1	1	1	0	1	0
1	1	1	0	1	0	1	1
1	0	1	0	1	1	0	0
1	0	1	1	1	1	0	1
1	0	0	1	1	1	1	0
1	0	0	0	1	1	1	1

Gray to binary conversion:



Understanding:

- The most significant digit in binary number is same as the corresponding digit in gray code.
- Each binary is added to generate the gray code digit in the next adjacent position.
- Gray to binary code converter circuit is implemented and its truth table is verified.

Post-lab Questions:

1. If X = '0100' the equivalent Gray code is
a. 0110 b. 1011 c. 1100 d. 0000
2. If X = '0011' is in Gray code, the equivalent Binary code is
a. 0110 b. 1011 c. 1100 d. 0000
3. While converting from Binary to gray code or vice –versa, the MSB
a. Is always '1' b. is always '0' c. is same as LSB
d. does not change
4. The logical gate used for constructing binary to gray code converter circuit is
a. AND b. NAND c. EX-OR d. NOR
5. The logical gate used for constructing gray to binary code converter circuit is
a. AND b. NAND c. EX-OR d. NOR

Result:

The conversion of BCD to Excess-3 and Gray Code to Binary is designed and verified using conversion table

10. Design of binary adder and Subtractor using IC's

Aim:

To design an adder and subtractor circuit to perform the following Arithmetic Operations.

- | | |
|-----------|--------------|
| i) $D+7$ | iii) $9E+FC$ |
| ii) $F-C$ | iv) $3C-1E$ |

Pre – lab Questions:

- 1) In a 4-bit adder, the LSB stage is always
 - a) fulladder
 - b) Ex-or
 - c) half-adder**
 - d) ANDgate
- 2) In a 4-bit adder, the final carry output is obtained
 - a) AtMSB**
 - b) atLSB
 - c) at each stage
 - d) none of the above
- 3) In a 4-bit adder, if the input operands are of 4-bits each, the composite output is
 - a) 4-bits
 - b)5-bits**
 - c)8-bits
 - d) 9-bits
- 4) One of the following statement is false:
 - a) Full adder has three outputs**
 - b) half-adder has two outputs
 - c) Full adder has three inputs
 - d) half-adder has two outputs

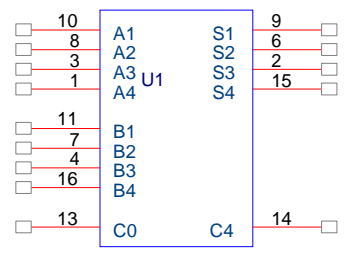
APPARATUS:

- 1) 2 Input Ex-Or Gates (74LS86) –2NO'S
- 2) 4 Bit Binary Adder(74LS83)-2NO'S
- 3) Digital IC TrainerKit
- 4) Logic Probes and Connecting Wires

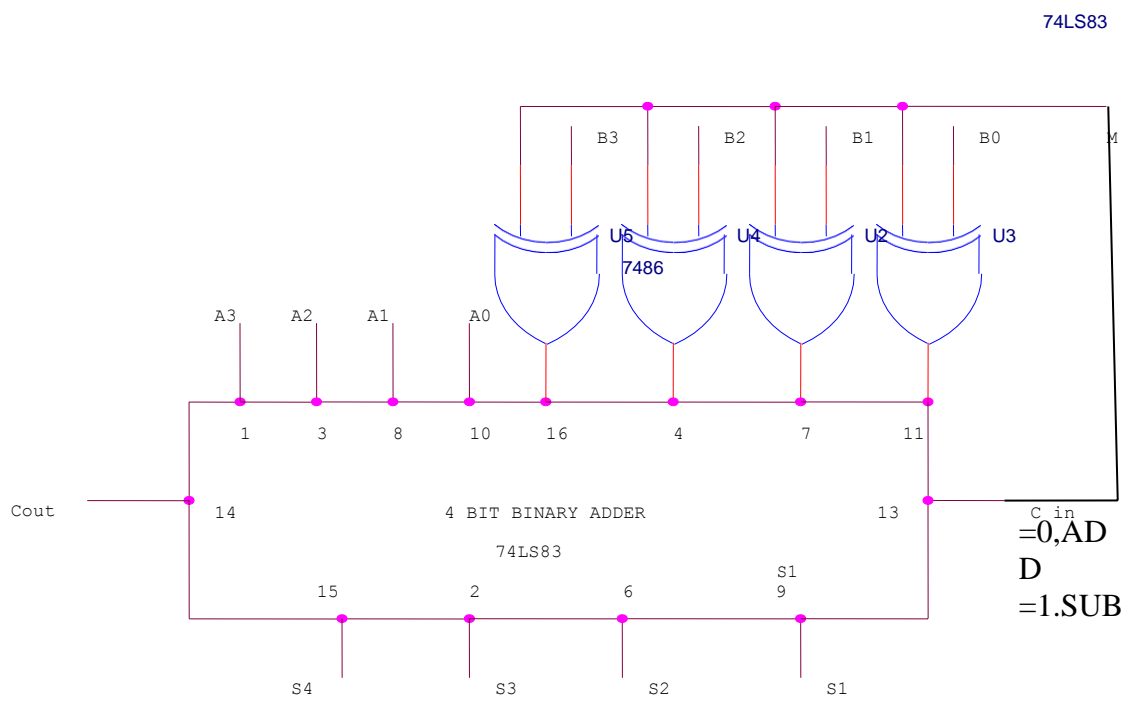
Theory:

- Two binary words each of n -bits can be added using a binary adder.
- Two Binary adders is a cascade of n full-adder stages each of which handles three bits (except LSB stage).
- The adder IC could be configured to implement subtraction also.

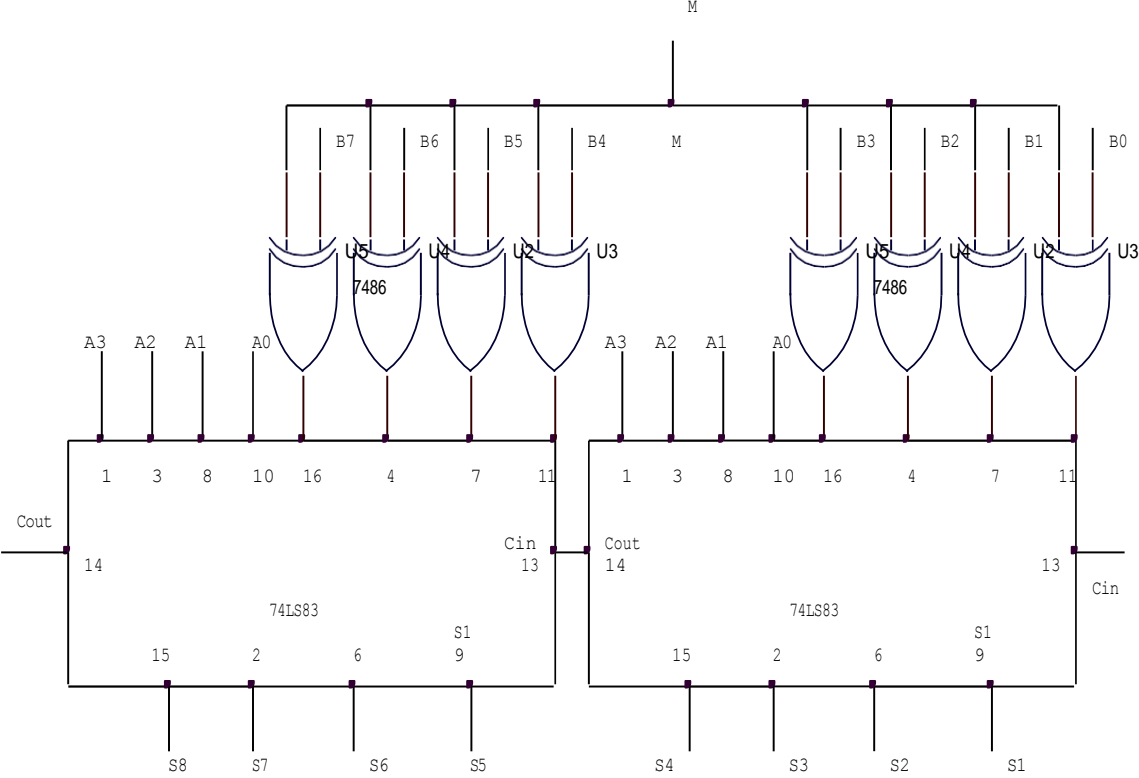
PIN DIAGRAM OF 74LS83



LOGIC CIRCUIT for 4-BIT RIPPLE CARRY ADDER SUBTRACTOR



LOGIC CIRCUIT FOR 8-BIT RIPPLE CARRYADDER SUBTRACTOR



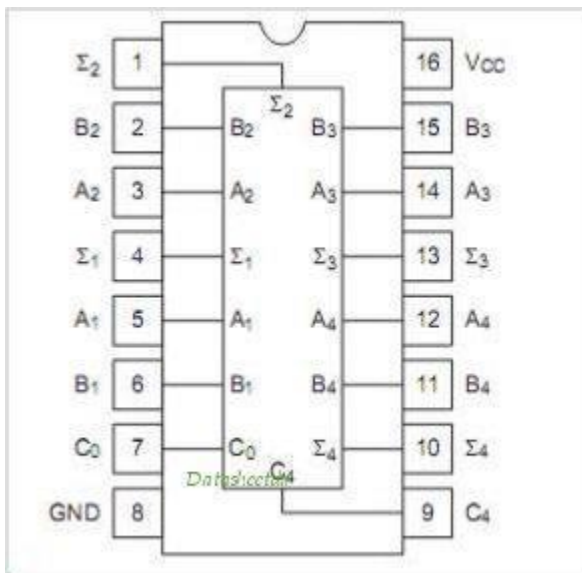
PROCEDURE:

4 BIT BINARY ADDER-SUBTRACTOR

- 1) Set the circuit of 7483 IC for addition ($D+7$) and 2's complement subtraction ($F-C$).
- 2) For addition operation the 'm' input is set '0' and the inputs D and 7 bits are set as a and b carry input 'c_{in}' is set '0'.
- 3) The result obtained is the sum of D and 7.
- 4) For subtraction operation the 'm' input is set '1' and the inputs F and C are fed as a and b the carry input 'c_{in}' is set as '1'.
- 5) The result is the 2's complement subtraction F-C.

8 BIT ADDERS AND SUBTRACTOR

- 1) Set the cascade circuit of two 4 bit Binary Adder (2no's Of 7483 ICs) as shown.
- 2) For addition operation the 'm' input is set '0' and the inputs 9e and Fc bits are set as a and b carry input 'c_{in}' is set '0'.
- 3) The result obtained is the sum of 9e and Fc.
- 4) For subtraction operation the 'm' input is set '1' and the inputs 3c and 1e are fed as a and b the carry input 'c_{in}' is set as '1'.
- 5) The result is the 2's complement subtraction 3c-1e



Understanding:

- 8-bit binary adder can be realized by cascading two 4-bit adders.

Post – lab Questions:

- 1) The adder circuit could be modified to realize subtraction by
 - a) using an array of OR gates

- b) **using an array of ex-orgates**
 - c) complementing both the operands
 - d) converting one operand into 1's complement and the other into 2's complement
- 2) To realize binary subtraction with adder circuit, the number system or arithmetic used is
- a) 1's complement b) BCD
 - c) 2's complement** d) excess-3
- 3) The binary adder could be modified to implement BCD subtraction if
- a) 1's complement is used
 - b) NOR gates instead of ex-or gates used for inverting each input bit
 - c) 9's complement is used
 - d) none of the above**

Result:

The given function was realized using 4-bit binary adder (74LS83) and values of the truth table was also verified

11. Design and implementation of Multiplexer and De-multiplexer using logic gates.

(i) Multiplexer

Aim:

To construct the circuit of multiplexer and to study their working

Pre – lab Questions:

- a. Multiplexer has n inputs and
 - a) One output
 - b) $2n$ output
 - c) n output
 - d) 2^n outputs

- b. Multiplexer is also called
 - a) Multiplier
 - b) Data selector
 - c) Data adder
 - d) Encoder

- c. The output is determined by
 - a) Select input
 - b) Highest input(MSB)
 - c) Lowest input(LSB)
 - d) All inputs

- d. If ' n ' is the number of select bits, the number of possible inputs are
 - a) $n!$
 - b) $\log n$
 - c) 2^n
 - d) n^2

- e. A multiplexer has ' m ' select bits, the number of outputs are
 - a) 0
 - b) 1
 - c) 2^n
 - d) $\log m$

Components required and their purpose

Component	Specification	Quantity	Purpose
NOT gate	74LS04 / 74HCT04	1	Combinational circuit element
3-input AND gate	74LS11 / 74HCT11	1	Combinational circuit element
2-input OR gate	74LS32 / 74HCT32	1	Combinational circuit element
Digital IC trainer kit		1	Construct the circuit in simple way

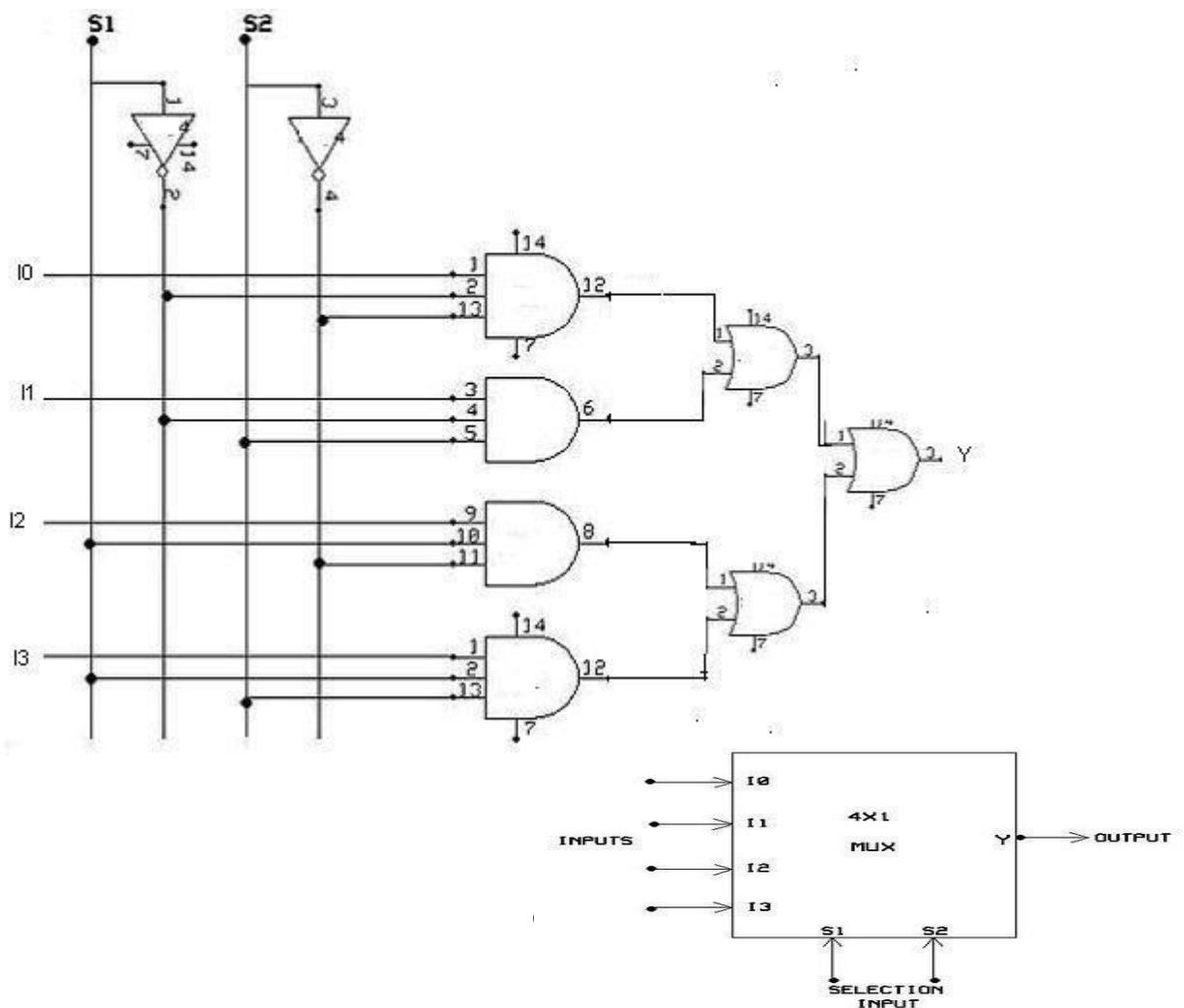
Theory:

- Multiplexer has many inputs and only one output.
- The selection of a particular input line is controlled by selectlines.
- Four inputs require 2 select lines ($n = 4, x = \log_2 n = 2$ selectlines).
- 4: 1 or 8: 1 or 16: 1 multiplexers are available as standard ICs.

Procedure:

1. Construct the circuit as shown in figure
2. Select the switches A, B, C and D to provide input bit combinations.
3. Select the switches X and Y to provide 'select'signals
4. Observe the output LED for each select input combination and verify the truthtable.

Logic Diagram:



Truth Table:

Select lines		Inputs				OUTPUT	Data line sent to output
S ₁	S ₂	I ₀	I ₁	I ₂	I ₃		
0	0	1	X	X	X	1	I ₀
0	1	X	1	X	X	1	I ₁
1	0	X	X	1	X	1	I ₂
1	1	X	X	X	1	1	I ₃

Understanding:

- Multiplexer has many inputs but always only one output.
- Data from only one of the available inputs is transferred to output at any given time.
- The input that is transferred to the output depends on the selection.

Post – lab Questions:

1. A multiplexer with 4 select bits can support upto
 - a) 4 inputs
 - b) 16inputs
 - c)One input
 - d) Any number of inputs
2. If there are 32 input bits the number of select bits requested are
 - a)5
 - b) 16
 - c)64
 - d) 32
3. To cascade multiplexers the control signal used is
 - a) Select
 - b) Strobe
 - c)Output
 - d) Any one of inputs
4. How many 2:1 multiplexers are required to realize 3:1 multiplexers?

- a) One
- c)Three

- b)Two
- d)Five

(ii) DeMultiplexer

Aim:

To construct the circuit of Demultiplexer and to study their working

Pre – lab Questions:

f. Demultiplexer is dual of

- a) Decoder
- c)Multiplexer**

- b)Full-adder
- d) Half-adder

g. Demultiplexer is also called

- a) Full-adder
- c)Tri-state buffer**

- b)Distributor**
- d) Converter

h. The number of output line(s) of a demultiplexer is/are

- a) One
- c)Many**

- b)Two
- d) Equal to input lines

i. The number of input to a demultiplexer is/are

- a) **ONE**
- c)Many

- b)Two
- d) Always at 'Z'

j. Demultiplexer is an example of

- a) Sequential logic
- c)Combinational logic**

- b) Memory circuit
- d) Data selector

Components Required:

Component	Specification	Quantity	Purpose
NOT gate	74LS04 / 74HCT04	1	Combinational circuit element
3-input AND gate	74LS11 / 74HCT11	1	Combinational circuit element
Digital IC trainer kit		1	Construct the circuit in simple way

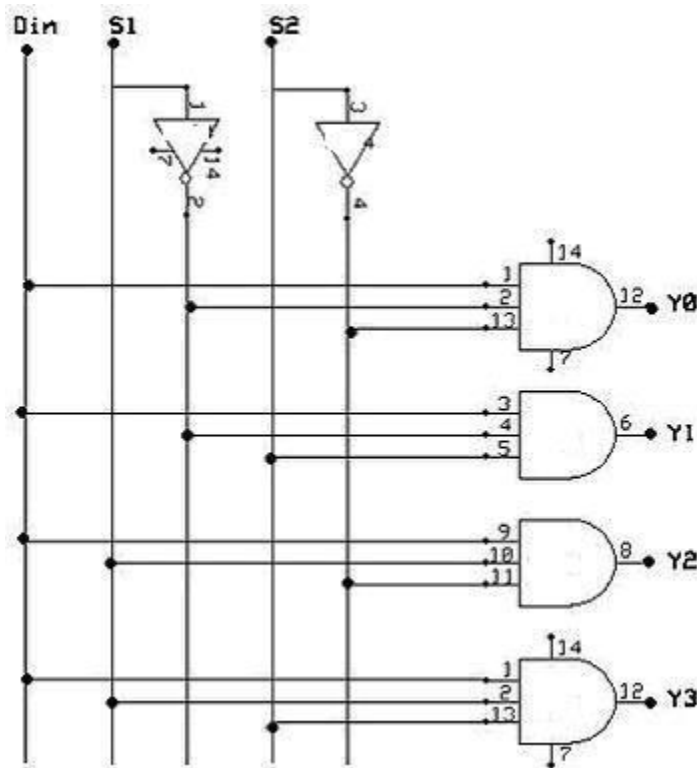
Theory:

- Demultiplexer has one input and many outputs.
- The selection of the particular output line is controlled by a set of control inputs called selectlines.
- For 1: n demultiplexer, the number of select lines required is $S = \log_2 n$ or $N = 2^S$.
- Four outputs require 2 select lines ($n = 4$, $S = \log_2 n = 2$ selectlines).

Procedure:

1. Construct the circuit as shown in figure
2. Select the switches A and B to provide input bit combinations.
3. Observe the output LEDs for each select input combinations and verify the truth table.

Logic Diagram:



Understanding:

- Demultiplexer has one input but many outputs.

- The selection of the particular output line is controlled by selectlines.
- Data input is transferred to only one of the outputs.
- The output that is transferred from the input depends on selectlines.

Truth Table:

Select input		Output			
S ₁	S ₂	Y ₀	Y ₁	Y ₂	Y ₃
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

Data input = '1'

Post – lab Questions:

- If 'n' is the number of outputs, the select lines required is/are

a) One	b) n
c) $\log_2 n$	d) 2^n
- If 'n' is the number of inputs the select lines required is/are

a) One	b) Does not depend on inputs
c) n	d) $\log n$
- The select bits to a de-multiplexer are 5, the number of possible output(s)is/are

a) 5	b) 1
c) 32	d) 16
- If the number of select bits are 4 the number of input line(s)is/are

a) 4	b) 2
c) 16	d) 1
- The demultiplexer can also be used as

a) Adder	b) Decoder
c) Subtractor	d) Buffer

RESULT:

Multiplexer and demultiplexer circuits were constructed and their operations were verified

12. Implementation and Testing of RS Latch and Flip-flops – D, JK and T.

Aim:

To verify the truth table of various flip-flops using logic gates

- i) R-S Flip-Flop
- ii) D-Flip-Flop
- iii) J-K Flip-Flop
- iv) T-Flip-Flop

i) R-S Flip-Flop

Pre-lab Test:

- The number of input(s) and output(s) respectively in a RS flip-flop is(are)
a) One,one b) one,two c) two,one **d) two,two**
- The condition that needs to be avoided in a RS flip-flop is
a) R=0, S=0 b) R=0, S=1 c) R=1, S=0 d) R=1, S=1
- When R=1 and S=1, the outputs
a) Toggle b) become '1'
c) Become '0' **d) do not change**
- The input combination required to set the output Q=1 is
a) R=1, S=1 **b) R=1, S=0** c) R=0, S=1 d) R=0, S=0

Components of the circuit and their purpose

Component	Specification	Quantity	Purpose
2 input NAND gate	74LS00 / 74HCT00	1	Circuit element
Digital IC trainer kit		1	Construct the circuit in simple way

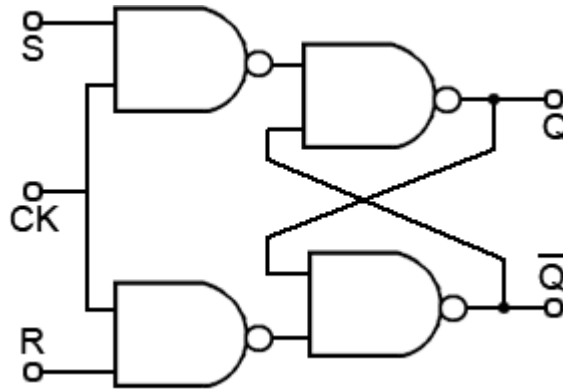
Theory:

- The RS flip-flop is an asynchronous sequential data storage circuit.
- It is formed by cross-coupling of two NAND/NOR gates.
- The cross-coupled connection from the output of one gate to the input of the other gate constitutes a feedback path.
- It has two outputs Q and Q' and two inputs, *set(S)* and *reset(R)*.
- The circuit is also called a direct-coupled RS flip-flop.

Procedure:

1. Construct the circuit as shown in figure
2. Select the switches S and R to provide input bit combinations.
3. Observe the LED output for each input bit combinations and verify the truthtable.

Logic diagram of Clocked SR-FF:



Truth Table:

INPUTS			OUTPUT	STATE
CLK	S	R	Q	
X	0	0	No Change	Previous
↑	0	1	0	Reset
↑	1	0	1	Set
↑	1	1	-	Forbidden

Understanding:

- When S= R=0, the NAND gates are disabled resulting in high output.
- When both S=R=1, the NAND gates are enabled and leaves the output in previous condition (hold).
- When S=0, R=1, the flip-flop is in set condition.
- When S=1, R=0, the flip-flop is in reset condition.
- RS flip-flop can also be constructed neither using NOR gates.
- RS flip-flop is an asynchronous circuit.
- It is made synchronous by adding a clock input.

Post Lab Questions:

1. The main drawback of the RS flip-flop is
 - a) Needs two NAND gates
 - b) needs feedback
 - c) Operates with a single clock
 - d) race condition**
2. The additional input that is used to avoid 'race' condition is
 - a) Clear
 - b)pre-set
 - c)clock**
 - d) strobe
3. The use of clock in RS flip-flop requires
 - a) One AND gate at each input**
 - b) two cross coupled AND gates
 - c) Additional stage of NAND gates
 - d) one NAND gate at each input

(ii)D- Flip-Flop

Pre-lab Test:

1. D flip-flop is equivalent to
 - a)RS latch
 - b) clocked RS latch**
 - c) cross-coupled NAND gate
 - d) cross coupled NORgate
2. The number of inputs to a D flip-flop is(are)
 - a)One**
 - b) two
 - c) three
 - d) four
3. The two outputs of a D flip-flop are
 - a) Same
 - b)complementary**
 - c)always1
 - d) always 0

Components of the circuit and their purpose

Component	Specification	Quantit y	Purpose
2 input NAND gate	74LS00	1	Circuit element
2 input NOT gate	74LS04	1	Circuit element
Digital IC trainer kit		1	Construct the circuit in simple way
NOT gate	74LS04	1	Circuit element

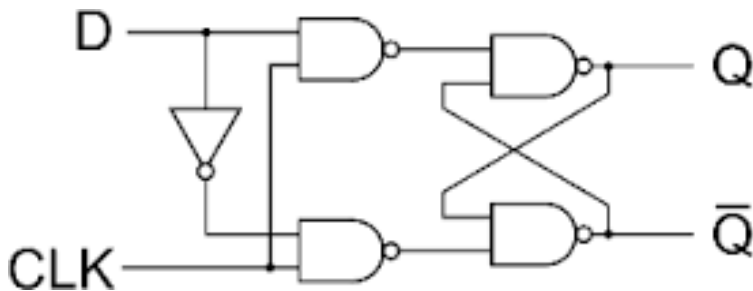
Theory:

- D flip-flop is a modified clocked RS flip-flop.
- It is formed from the clocked RS flip-flop by the addition of an inverter in the R input.
- The added inverter reduces the number of inputs from two to one.
- This flip-flop is also called a gated D-latch.

Procedure:

1. Construct the circuit as shown in figure using *spice* tool.
2. Select the switches D and C to provide input bit combinations.
3. Observe the LED output for each input bit combinations and verify the truth table.

D-Flipflop



Understanding:

- The D input is sampled during the occurrence of a clock pulse.
- The pulse of '0', switches the flip-flop to the clear state.
- D flip-flop (data flip-flop) has the ability to transfer 'data' into the succeeding flip-flop.
- D flip-flop can be constructed using J-K flip-flop.

Truth Table:

CLOCK	D	Q _{n+1}
0	0	Q _n = (No change)
0	1	Q _n = (No change)
1	0	0
1	1	1

Post Lab Questions:

1. The main application of D flip-flop circuit is in
a) Address **b) shift registers** c) multiplexers d) counters
2. In a D flip-flop, constructed using JK flip-flop
a) J and K are given same inputs **b) J and K have complementary inputs**
c) J should be '1' and K should be 'don't care' d) J = '0' and K = 'X'

iii) J-K Flip-Flop

Pre – lab Questions:

1. The JK flip-flop is also called as
a) RS flip-flop b) D flip-flop
c) Gated RS flip-flop d) gated T flip-flop
2. In a JK flip-flop, when J=1, the other input 'K' should be _____ for the output to be '1'.
a) '0' b) '1' c) 'X' d) 'Z'
3. When both the inputs J and K are equal, the output
a) becomes '1'
b) becomes '0'
c) changes depending upon whether the input is a '1' or '0'
d) remains in the previous state
4. The asynchronous inputs in a JK flip-flop are
a) J and K only b) clock and clear
c) J, K and clock **d) preset and clear**
5. In a JK flip-flop, if both inputs J and K are '0', the output 'Q'
a) becomes '1' b) becomes '0'
c) Toggles **d) remains in the previous state**

Components of the circuit and their purpose:

Component	Specification	Quantity	Purpose
3 input NAND gate	74LS10	1	Circuit element
Digital IC trainer kit		1	Construct the circuit in simple way
2 input NAND gate	74LS00	1	Circuit element

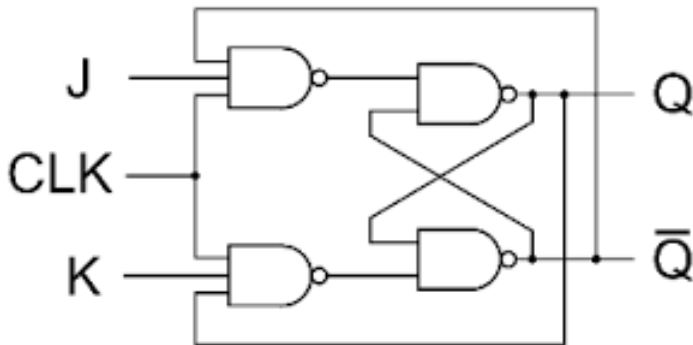
Theory:

- JK flip-flop performs three operations: set to '1', reset to '0' or complement its output.
- The J input sets the flip-flop to '1', the K input resets it to '0' and when both inputs are enabled, the output is complemented.

Procedure:

1. Construct the circuit as shown in figure.
2. Select the switches J and K to provide input bit combinations.
3. Observe the output LED for each input bit combinations and verify the truthtable.

Circuit diagram:



Truth Table:

CLOCK	J	K	Q_{n+1}	$(Q_{n+1})^I$	Condition
0	X	X	Q_n	Q_n^I	No change
1	0	0	Q_n	Q_n^I	No change
1	0	1	0	1	Reset
1	1	0	1	0	Set
1	1	1	Q_n^I	Q_n	Toggle

Understanding:

- When $J=0$ and $K=1$, the next clock resets the output to '0'.
- When both $J=K=1$, the next clock complements the output.
- When $J=K=0$, the next clock leaves the output unchanged.
- When J and K inputs are tied together, JK flip-flop forms a T flip-flop.
- When J and $K=J'$, JK flip-flop becomes D flip-flop.
- In master-slave JK flip-flop, the output will be activated during the clock edge instead of clock level as in case of JK flip-flop.
- Most of JK flip-flop ICs incorporate JK master-slave configuration only.

Post – lab Questions:

1. In the JK-FF, when a '0' is applied to the *pre-set* input, the Q' output, is
a) '0' b) '1'
c) Cannot be determined unless J input is specified
d) Cannot be determined unless K input is specified.

2. Both pre-set and clear are called
a) Control inputs b) enable inputs
c) **Asynchronous inputs** d) synchronous inputs

3. Given $J=K='1'$. When '1' is applied to the *clear* input, the output Q,
a) is set to '1' b) toggles
c) is set to '0' d) **remains in the previous state**

4. The symbol ' \uparrow ' in a JK M-S flip-flop indicates that
a) clock is true b) **clock changes from '0' to '1'**
c) Clock is false d) clock changes from '1' to '0'

5. The symbols ' \uparrow ' and ' \downarrow ' indicate that the JK-FF is
a) **Edge triggered** b) level triggered
c) Does not depend on clock d) the outputs do not depend on clock

iv) T-Flip-Flop

Pre-lab Test:

1. A T flip-flop is constructed using
a) RS flip-flop b) RS latch c) D latch **d) JK flip-flop**
2. In T flip-flop, to cause an output to change, input is
a) Always '0' **b) always '1'**
c) Complementary d) independent of clock
3. The main application of T flip-flop is in
a) Counters b) shift registers c) adder d) multiplexer
4. The clock input in a T flip-flop should always be _____ to cause a change in the output
a) true b) raising c) falling **d) either (b) or (c)**

Components of the circuit and their purpose

Component	Specification	Quantity	Purpose
2 input NOR gate	74LS02 / 74HCT02	1	Circuit element
3 input AND gate	74LS11 / 74HCT11	1	Circuit element
Digital IC trainer		1	Construct the circuit in simple way

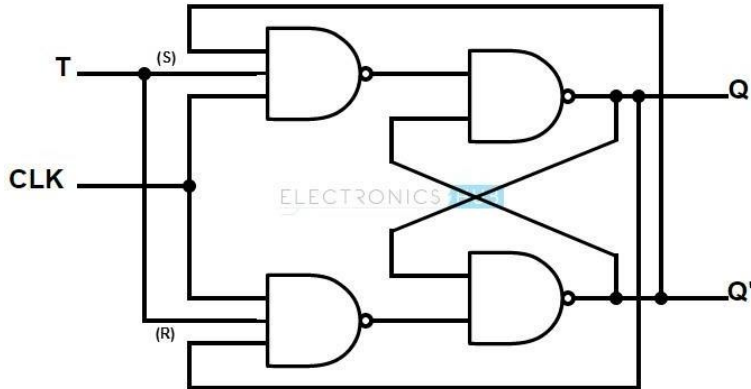
Theory:

- The T flip-flop is a single input version of the JK flip-flop.
- It is obtained from a JK type if both inputs are tied together.
- T stands for toggling of the state at the output.
- When T is held high, the flip-flop divides the clock frequency by two.
- This "divide-by" feature has application in various types of digital counters.

Procedure:

1. Construct the circuit as shown in figure
2. Select the switches T and C to provide input bit combinations.
3. Observe the output LED for each input bit combinations and verify the truth table.

T-Flip flop:



Truth Table:

clock	T	Q _{n+1}	(Q _{n+1}) ^I
0	X	no change	0
1	0	1	0
1	1	0	1

Understanding:

- The output of the T flip-flop "toggles" with each clock pulse when T='1'.
- A T flip-flop can also be realized using an RS flip-flop and D flip-flop.

Post Lab Questions:

1. One of the following statements is false in a T flip-flop

- a) There are two inputs and two outputs b) the T flip-flop is always edge triggered
c) One of the outputs is fed back to J input d) J and K inputs are tied together

2. To convert a T flip-flop into a D flip-flop, the following change needs to be made

- a) Same inputs applied separately to J and K b) The clock level should always be '1'
c) Complementary inputs applied to J and K d) The clock level should always be '0'

3. When T flip-flops are cascaded,

- a) Outputs of a previous stage are connected to J and K inputs of next stage respectively
b) The Q output is connected to K input of next stage
c) The Q' output is connected to J input of next stage
d) The Q output connected to clock input of next stage

RESULT:

Thus the truth table of various flip-flops like i) R-S Flip-Flop ii) D-Flip-Flop iii) J-K Flip-Flop iv) T-Flip-Flop were verified using logic gates

13. Design of synchronous counter

Aim:

To Design A Mod 6 Synchronous Counter Using J-K Flip-flops.

Pre-lab Test:

- The main advantage of synchronous counters is (are)that
 - It minimizes the effect of glitches**
 - it uses fewer number of flip-flop stages
 - Requires a single power supply
 - none of the above
- The clock in a n-bit synchronous counter is applied
 - At the MSB stage
 - at the LSB stage
 - At each stage in parallel**
 - at (n-1)th stage
- A modulo-5 counter has stages from (in binary)
 - '000'to '100'**
 - '001' to'101'
 - '000'to '101'
 - '001' to'100'
- One of the following is not a counter.
 - Modulo
 - ripple
 - ring
 - mealy**
- The main requirement of a ring counter is that
 - The clock is applied to the LSB stage
 - The clock is applied to the MSB stage
 - All the flip-flops are reset at start**
 - All the flip-flops are set at start

APPARATUS:

- J-K Flip-Flop (74LS73) –2
- 2-Input Quad AND Gate (74LS08) –1
- Digital IC TrainerKit
- Logic Probes and Connecting Wires

Excitation Table for J – K Flip-Flop:

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Present state			Next state			Excitation Values					
QC	QB	QA	QC	QB	QA	JC	KC	JB	KB	JA	KA
0	0	0	0	0	1	0	X	0	X	1	X
0	0	1	0	1	0	0	X	1	X	X	1
0	1	0	0	1	1	0	X	X	0	1	X
0	1	1	1	0	0	1	X	X	1	X	1
1	0	0	1	0	1	X	0	0	X	1	X
1	0	1	0	0	0	X	1	0	X	X	1
1	1	0	1	1	1	X	X	X	X	X	X
1	1	1	0	0	0	X	X	X	X	X	X

Minimization:

$QBQA$	$\overline{Q_B}\overline{Q_A}$	$\overline{Q_B}Q_A$	$Q_B\overline{Q_A}$	Q_BQ_A
QC	1	X	X	1
Qc	1	X	X	X

$$J_A = 1$$

$QBQA$	$\overline{Q_B}\overline{Q_A}$	$\overline{Q_B}Q_A$	$Q_B\overline{Q_A}$	Q_BQ_A
QC	X	1	1	X
Qc	X	1	X	X

$$K_A = 1$$

$QBQA$	$\overline{Q_B}\overline{Q_A}$	$\overline{Q_B}Q_A$	$Q_B\overline{Q_A}$	Q_BQ_A
QC	0	1	X	X
Qc	0	0	X	X

$$J_B = \overline{Q_C}Q_A$$

$QBQA$	$\overline{Q_B}\overline{Q_A}$	$\overline{Q_B}Q_A$	$Q_B\overline{Q_A}$	Q_BQ_A
QC	X	X	1	0
Qc	X	X	X	X

$$K_B = Q_A$$

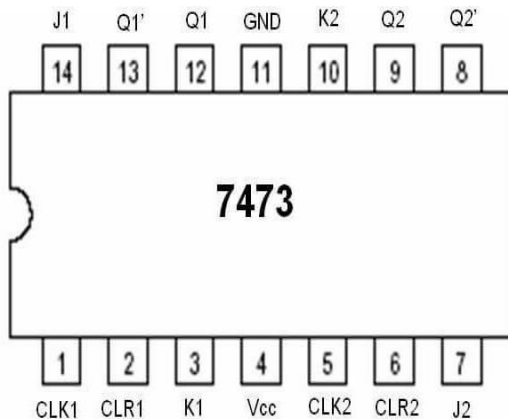
$QBQA$	$\overline{Q_B}\overline{Q_A}$	$\overline{Q_B}Q_A$	$Q_B\overline{Q_A}$	Q_BQ_A
QC	0	0	1	0
Qc	X	X	X	X

$$J_C = Q_AQ_B$$

$QBQA$	$\overline{Q_B}\overline{Q_A}$	$\overline{Q_B}Q_A$	$Q_B\overline{Q_A}$	Q_BQ_A
QC	X	X	X	X
Qc	0	1	X	X

$$K_C = Q_A$$

Pin diagram:



Understanding:

- In parallel counters, all of the flip-flops will change states simultaneously.
- The propagation delays of the flip-flops do not add together to produce the overall delay.

Post Lab Questions:

1. In a synchronous counter, which of the following statement is false?
 - a) The 'preset' and 'clear' inputs are asynchronous
 - b) The 'preset' and 'clear' inputs are connected to Vcc for normal operation
 - c) The decoding gates in between any two stages are similar**
 - d) The clock is applied simultaneously to all stages

2. The decoding gates used in between any two stages are required to
 - a) Transfer Q output to next stage
 - b) Transfer Q' output to next stage
 - c) Maintain clock synchronization
 - d) Reset the flip-flop upon reaching the desired count**

3. In a modulo-10 down counter, the initial state of count is
 - a) '0000'
 - b) '1001'**
 - c) '1111'
 - d) '1010'

4. An up/down counter is set or reset to a pre-determined state with the use of
 - a) 'Preset' only
 - b) 'clear' only
 - c) Either 'preset' or 'clear' inputs as required**
 - d) clock signal

5. When the preset inputs of all flip-flops in a 5-bit counter are momentarily connected to 'GND', the state of counter is
- a) '00000' b) '11111' c) '10000' d) '00001'

Result:

The operation of Mod 6 Synchronous Counter was verified Using J-K Flip-flops

14. Design of asynchronous counter

Aim:

To design a 4 - bit ripple counter, and to display their logic states.

Pre – lab Questions:

1. In an asynchronous counter, each of the successive flip-flop is triggered by
 - a) Applying a '1' at 'J' input
 - b) applying a '0' at 'k' input
 - c) Pulling 'clear' input of each flip-flop 'high'
 - d) the previous flip-flop**
2. A 4-bit counter requires _____ flip-flop
 - a) 2
 - b) 4**
 - c) 3
 - d) 5
3. In a 4-bit counter, the maximum count obtained is (in binary)
 - a) '1001'
 - b) '1100'
 - c) '1111'**
 - d) '0111'
4. The main drawback of the asynchronous counter is the
 - a) Need a flip-flop for each stage
 - b) delay**
 - c) Requirement of additional power supply
 - d) the need for a common clock
5. The limitation of asynchronous counter could be overcome by using
 - a) Parallel configuration
 - b) serial-parallel configuration**
 - c) Additional flip-flop stages
 - d) additional power supply

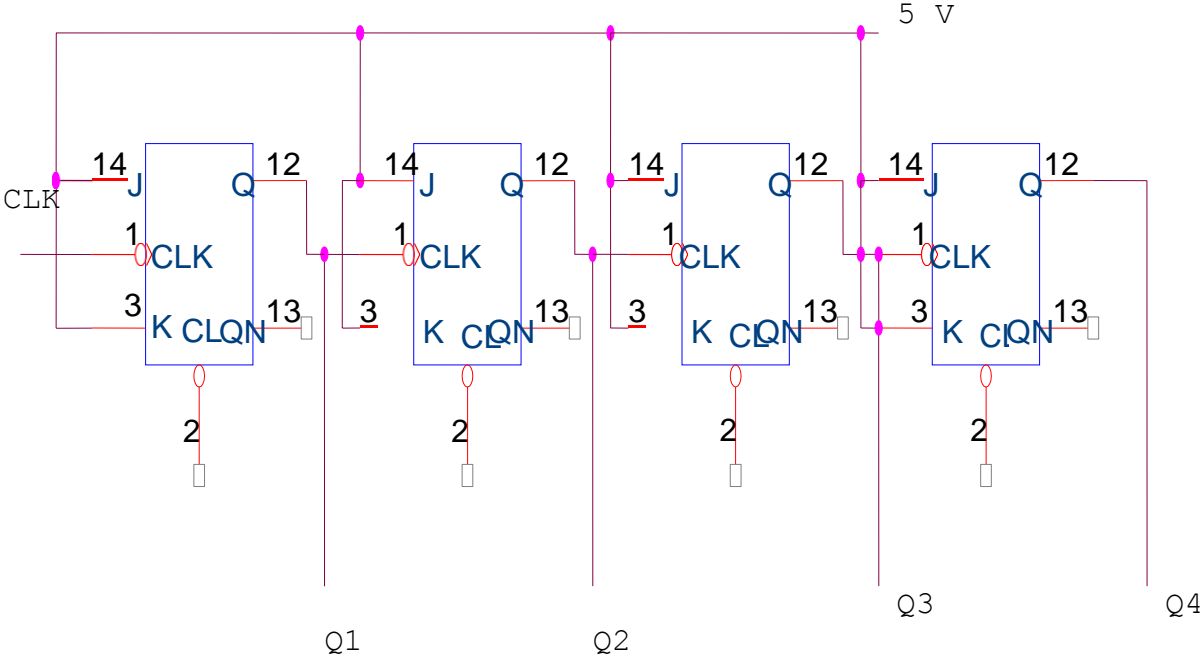
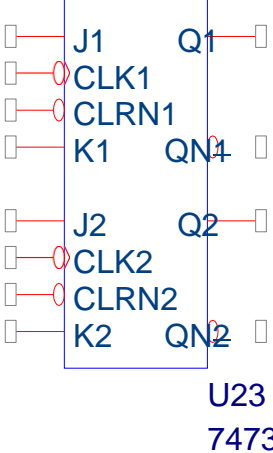
APPARATUS:

- 1) Dual J– K FLIP-FLOPS (7473) –2NOS
- 2) Quad 2-Input NAND Gate 7400 –1
- 3) Digital IC Trainer Kit
- 4) Logic Probes and Connecting Wires

PIN DIAGRAM:

7490(0-9) Ripple counter
7493(0-15) Ripple counter

PIN DIAGRAM

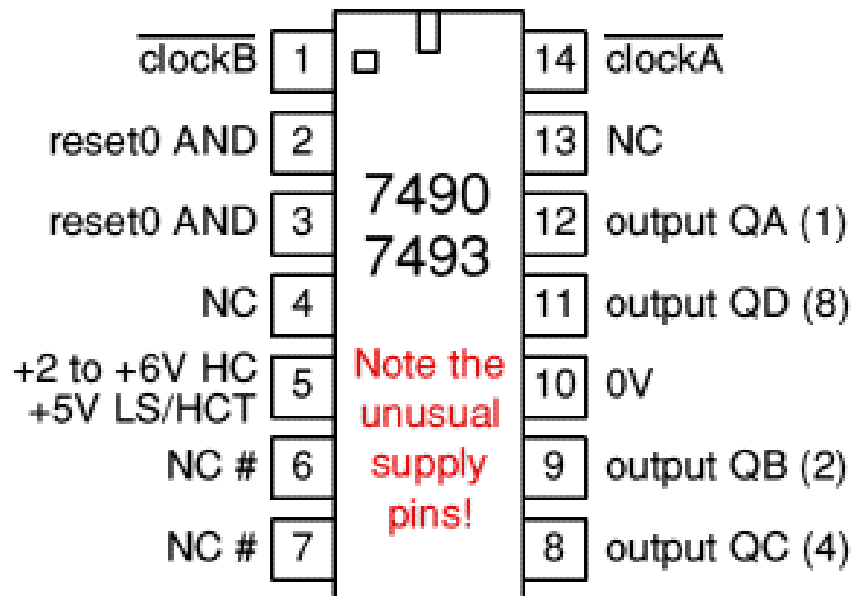


4 BIT RIPPLE SYNCHRONOUS COUNTER

TRUTH TABLE

CLK PULSE	Q4	Q3	Q2	Q1
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

PIN DIAGRAM:



PROCEDURE:

1. Circuits are connected as shown in figure.
2. By applying the clock the waveforms of Q_0 , Q_1 , Q_2 And Q_3 are observed In C.R.O

PRECAUTIONS:

- Avoid loose and wrong connections.
- Handle the equipment carefully.

Post – lab Questions:

1. The IC that is required to construct counter is
 - a) Latch
 - b) flip-flop**
 - c) multiplexer
 - d) decoder
2. If the JK flip-flop is used in the construction of counter, the JK is configured as
 - a) D flip-flop
 - b) JK master-slave
 - c) T flip-flop**
 - d) JK flip-flop itself but with $J=K=0$
3. In a modulo-9 up-counter, once the last count sequence is reached, the next count sequence is
 - a) '1001'
 - b) '1010'
 - c) '1111'
 - d) '0000'**
4. To construct a modulo-n up counter, the Q output of one stage is
 - a) connected to the 'J' input of the next stage
 - b) connected to the 'K' input of next stage
 - c) connected to the 'clock' input of the next stage**
 - d) left unconnected
5. To convert an up-counter to a down-counter,
 - a) the Q output is connected to 'K' input of next stage
 - b) the Q' output is connected to the clock input of next stage**
 - c) the Q' output is connected to the J input of next stage
 - d) the Q output is connected to the clock input of next stage

Result:

The operation of 4 bit ripple counter was verified using J– K FLIP-FLOPS

Experiments beyond the Syllabus (Mini Projects)

EXP 1: <https://circuitdigest.com/555-timer-circuits> (Using 555 timer)

EXP2: <https://circuitdigest.com/op-amp-circuits> (Using op-amp)

EXP 3: <http://www.circuitstoday.com/7-segment-counter-circuit> (Using analog and Digital IC's)